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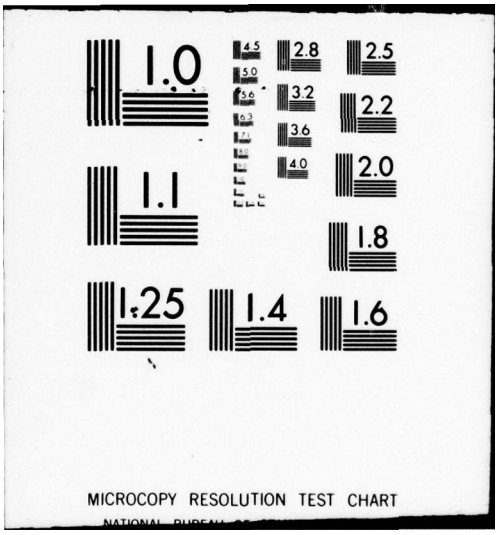
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LEVEL II

RADC-TR-79-130
Final Technical Report
June 1979

CHARACTERIZATION OF MICRO-PROCESSORS AND MICROPROCESSOR SUPPORT CHIPS

General Electric Company

Thomas M. Ostrowski

ROME AIR DEVELOPMENT CENTER
Air Force Systems Command
Griffiss Air Force Base, New York 13441

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APPROVED: Regis C Hilow

REGIS C. HILOW
Project Engineer

APPROVED: Joseph J Naresky

JOSEPH J. NARESKY
Chief, Reliability and Compatibility Division

FOR THE COMMANDER: John P. Huss

JOHN P. HUSS
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(19) REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
(18) 1. REPORT NUMBER: RADC-TR-79-130 / 2. GOVT ACCESSION NO.	3. RECIPIENT'S CATALOG NUMBER
4. TITLE (and Subtitle): (6) CHARACTERIZATION OF MICROPROCESSORS AND MICROPROCESSOR SUPPORT CHIPS	5. TYPE OF REPORT & PERIOD COVERED: (9) Final Technical Report Jan 78 - Sep 78
	6. PERFORMING ORG. REPORT NUMBER: N/A
7. AUTHOR(s): (10) Thomas M. Ostrowski	8. CONTRACT OR GRANT NUMBER(s): (15) F30602-77-C-0012
9. PERFORMING ORGANIZATION NAME AND ADDRESS: General Electric Company, 100 Plastics Avenue, Pittsfield MA 01201	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: (16) 62702F 23380118 (17) 01
11. CONTROLLING OFFICE NAME AND ADDRESS: Rome Air Development Center (RBRM), Griffiss AFB NY 13441	12. REPORT DATE: (11) June 1979
	13. NUMBER OF PAGES: 84
14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office): Same (12) 93 p.	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

Same

18. SUPPLEMENTARY NOTES

RADC Project Engineer: Regis C. Hilow (RBRM)

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Microprocessor
Support Devices
Test Methods
Electrical Testing
MIL-M-38510 Slash Sheets

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of this effort was to develop high test confidence level functional tests and parametric tests for selected microprocessors and microprocessor support devices; and then generate MIL-M-38510 slash sheets for them which conformed to military standards. This included worst case test situations, critical timing and generation of new test procedures where present or accepted methods no longer apply. Devices characterized were the 1802 CMOS microprocessor, 8228/38 system controller and bus driver, 8224 clock generator and driver and 6821 peripheral interface adapter.

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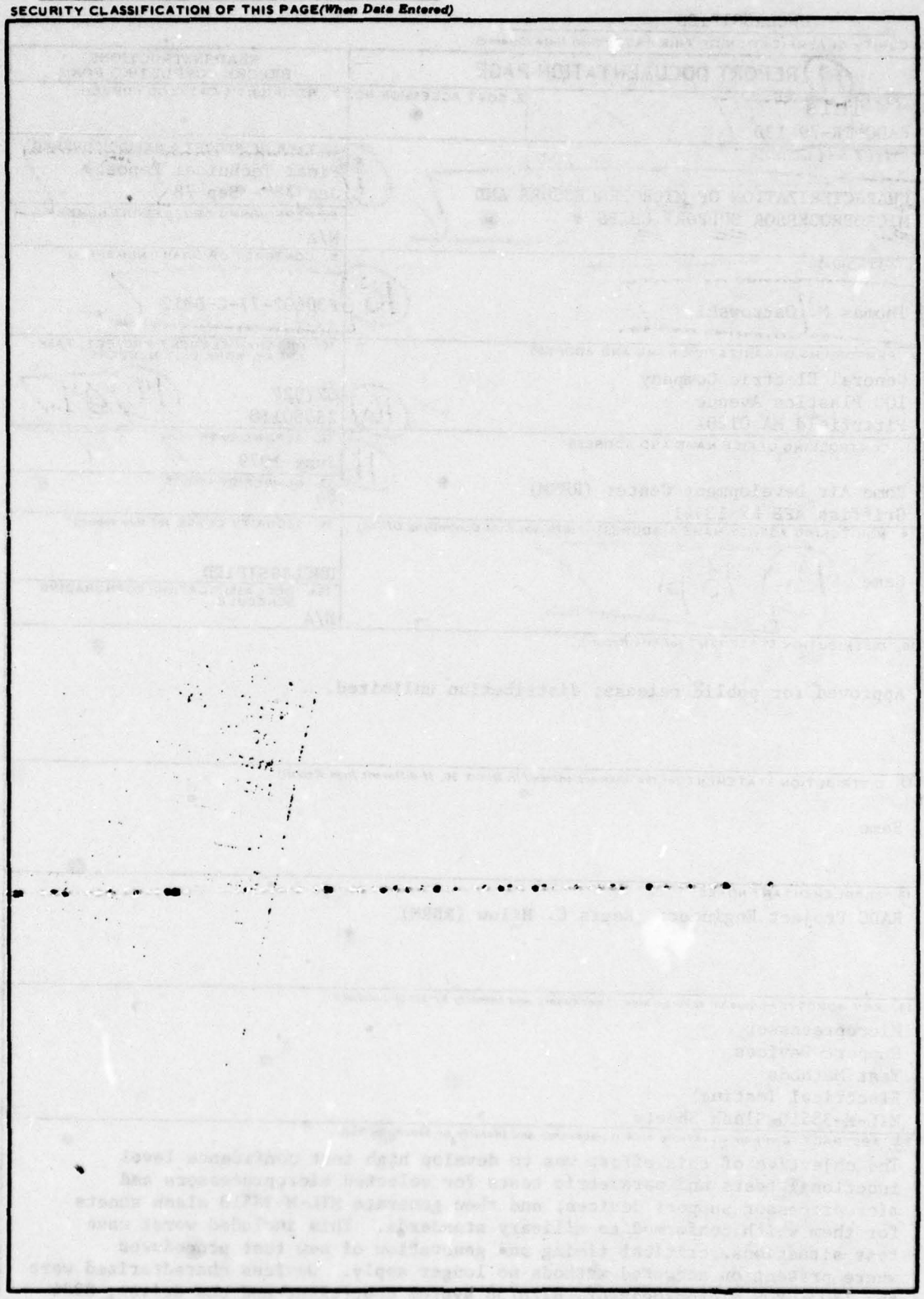

PREFACE

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This Final Report was prepared by General Electric Ordnance Systems, 100 Plastics Avenue, Pittsfield, Massachusetts, for Rome Air Development Center, Griffiss Air Force Base, New York, under contract F30602-77-C-0012. It covers the period January 1978 to September 1978. Mr. Regis C. Hilow, RBRM, was the RADC Project Engineer.

The work of this project was performed by the Electronic Circuits Engineering Operation and Components Engineering Unit. Project responsibility was held by Mr. Thomas Ostrowski of Circuit Design Engineering. Key individuals who made significant contributions to this report were Messrs. Barney Hajduk, Larry Roller, Richard English, Lawrence DeLuca, Winston Taylor, David Prystasz and Clarence Carey.

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EVALUATION

The objective of this study was to electrically characterize microprocessors and various support devices over the defined temperature range of -55°C to +125°C. This includes assurance that the devices studied are technically accurate and function as designed.

To satisfy the above objective, the devices selected were tested under worst case loading, critical timing and worst case instruction sequences or test patterns. The prime microprocessor studied in this effort was the 1802 CMOS 8-bit fixed instruction device. This electrical characterization was undertaken to assure that the vector sets, used by RCA and NASA in preparing the initial military specification, gave a high testing confidence level and satisfied the test philosophy incorporated into other military (JAN) microprocessor specifications. This report contains detail of this comparison and general conclusions.

The support devices studied in this effort were the 8228/8238 system controllers, the 8224 clock generator and the 6821 peripheral interface adapter. These devices are used in systems with the JAN qualified 8080A and 6800 microprocessors. Draft JAN specifications were prepared as result of this work.

RADC, as Preparing Activity of MIL-M-38510, General Specification for Microcircuits, is responsible for managing the development and preparation of detail slash sheets for this specification. This study and future studies will be expanded in the microprocessor area and accelerated to provide DoD system builders with state-of-the-art devices specified to meet military environmental requirements.

Regis C. Hilow

REGIS C. HILOW
Project Engineer

SECTION I

SUMMARY

This report details a gate-level functional analysis performed on a microprocessor and microprocessor support devices. These results were used in the generation of MIL-M-38510 slash sheets (not included here). The characterized devices are listed below.

The microprocessor test philosophy used for this effort was established on previous contracts with RADC and was further developed and reported on in RADC report RADC-TR-78-138 June 1978 as a "Procedure For LSI Functional Test Development".

During this reporting period a similar characterization effort was in progress on one of the same devices being characterized on this program (1802 CMOS microprocessor). Included in this report is a comparison of the resulting test patterns of both programs and a comparison of the test philosophies.

Appendices to the report include pertinent test programs and test patterns also developed on this contract.

Characterized Devices

1802 CMOS 8-bit Microprocessor

8228/8238 System Controller and Bus Driver

8224 Clock Generator and Driver

6821 Peripheral Interface Adapter (Partial)

SECTION II

INTRODUCTION

Objective and Background

The characterization reported on herein is a continuation of similar effort transacted on this contract for RADC (F-30602-77-C-0012) and reported on in RADC report RADC-TR-78-138.

The objective of this program was to generate MIL-M-38510 slash sheets for selected microprocessors and support devices. New devices were selected for characterization primarily on the basis of military need. Also, where there was a similar need, established slash sheet processor families were augmented with additional support devices. Unguided proliferation of microprocessors is undesirable because of the extensive software support requirements and the need to additionally characterize companion support devices. These support devices can be more complex than the processor itself.

The functional test development philosophy that was used consisted primarily of partitioning large functions into basic functional blocks such as registers and multiplexers and then developing tests using proven test techniques (the detailed test development philosophy is documented in the RADC report previously mentioned in this section). Close coordination with manufacturers was maintained in order to facilitate test development and to ultimately provide a more practical test. All of the test development was based upon actual logic and detailed functional block diagrams supplied by manufacturers. This results in a very efficient and comprehensive test. In some cases manufacturer supplied tests were analyzed, augmented where necessary, and made to comply with the established test philosophy. The slash sheets were developed to provide tests that are independent of automatic tester types and are consistent with established military standards.

SECTION III

TEST DEVELOPMENT FOR THE 1802 CMOS MICROPROCESSOR

Introduction

The purpose of this section is to describe the functional tests developed for use in the MIL-M-38510 slash sheet for the CDP 1802 microprocessor (1470). The approach used in developing these tests consisted of separating the microprocessor into functional blocks and ensuring that the gate level circuitry in each block was verified. The "Procedure for LSI Functional Test Development" developed for RADC on this contract and documented in Report RADC-TR-78-138, June 1978 was used as a guideline. Functional test patterns received from Vendor E, the original source for the 1802, were used as the basis of the analysis. Vectors were inserted and revised, and sections of patterns completely replaced in the development of the tests described in the following report.

Summary

Tests developed by Vendor E were used so that, in addition to reducing test generation time, any known processor sensitivity checks put in by Vendor E and not readily apparent to users would be checked. The tests received from Vendor E consisted of 5000 vectors for verifying the scratch pad memory and 2500 vectors for verifying the remaining logic functions. Originally, it had been planned to spot check the vectors and review Vendor E's test philosophy to determine if they were performing the types of tests required to verify each functional block.

Investigation into Vendor E's vectors revealed that all functional blocks were not tested as thoroughly as initially anticipated. After further investigation, Vendor E was contacted to discuss problem areas. Personnel who developed these tests were no longer at Vendor E so the test strategy used in developing the tests was not clearly known. A thorough investigation of Vendor E's vectors was subsequently performed. It showed that the test patterns did not completely verify the functional blocks of the microprocessor. Tests for the scratch pad memory were rewritten and other tests were inserted into or appended to the control logic tests.

At the time of this analysis there were only two second sources for the 1802 microprocessor. Both second sources had full mask agreements which meant that Vendor E's gate level implementation would be used in manufacturing this device.

Therefore, test development was based upon Vendor E's gate level implementation. Any variation from this implementation would require investigating the revision at the gate level to determine the testing effectiveness of the existing tests.

A listing of the test patterns developed is included in Appendix E.

Test Development for The CDP 1802 Microprocessor

Tests developed by Vendor E for the CDP 1802 microprocessor were investigated. It was found that portions of the microprocessor were not completely verified by these tests. Additional vectors were generated to complete the verification of functional blocks with proven test patterns.

The 1802 microprocessor was divided into functional blocks, and each block was analyzed. The microprocessor was initially separated into the functional blocks defined in the block diagram from Vendor E's specification shown in Figure 3-1. The control logic block was further partitioned into specific functions. The main divisions of the control logic consisted of: Timing Circuitry, I Decoders, N Decoder, Conditional Short/Long Branch/Skip Logic, Register Control Logic, and I/O Interrupt Servicing Logic.

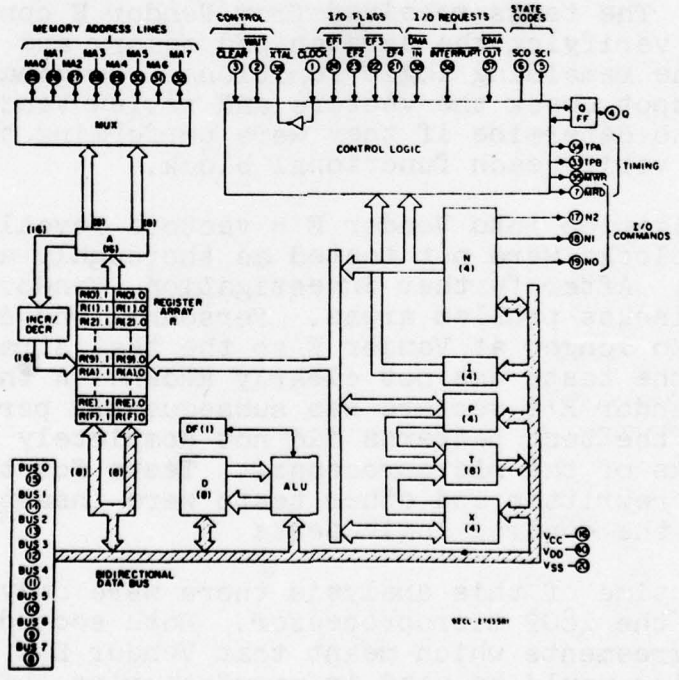


Figure 3-1. CDP1802 block diagram

1802 Scratch Pad Memory Test (Test Sequence SP)

The scratch pad memory (SPM) in the CDP 1802 microprocessor consists of a 16 x 16 bit register array. Each of the 16 bit registers is selected by a 4 to 16 bit decoder. Once selected all 16 memory bits of the register are enabled for either the read or write operation.

Register array verification is accomplished by ensuring register independence, bit independence, and integrity of unique registers. Register independence is verified by writing into one of the registers and checking that the others are not affected. Bit independence is shown by having each bit in a zero and one state while other bits are in the complemented state, not necessarily all at once, sometime in the testing sequence.

Each scratch pad memory cell (bit) in the 1802 contains two cross-coupled inverters which form a flip-flop storage element as shown in Figure 3-2. Single transistor transmission gates are employed to perform the sensing and storing operations in the storage-cell selection.

Tests which verify the operation of the scratch pad memory cell must ensure that both the cross-coupled inverters and the transmission gates are functioning correctly. The cross-coupled inverter operation is ensured by writing a logic "1" over a logic "0" and writing a logic "0" over a logic "1" (integrity).

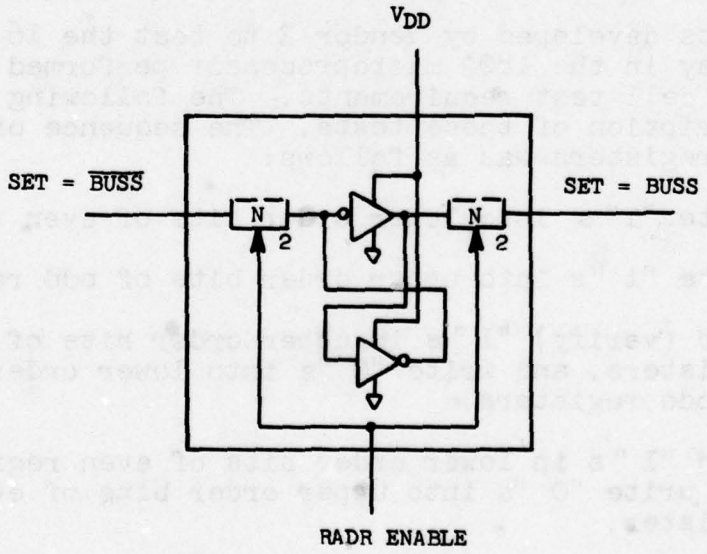


Figure 3-2. Scratch pad memory cell

Test requirements for transmission gates must ensure that the gate will:

1. Transmit a logic "1"
2. Transmit a logic "0"
3. Present a high impedance for a 0, 1 and 1, 0 condition.

Based upon this philosophy, the tests required to ensure that each cell in the scratch pad memory is functioning correctly are as follows:

1. Write a logic "1" over a logic "0".
2. Write a logic "0" over a logic "1".
3. Read a logic "1" out of the memory cell when a logic "0" previously existed on this Bus line.
4. Read a logic "0" out of the memory cell when a logic "1" previously existed on this Bus line.

The first two tests ensure that the memory cell will transmit and latch logic levels "1" and "0". Tests three and four verify the bidirectional high impedance operation of the memory cell.

Evaluation of Vendor E's Tests for Scratch Pad Memory

The tests developed by Vendor E to test the 16 x 16 bit register array in the 1802 microprocessor performed some of the above memory cell test requirements. The following section gives a brief description of these tests. The sequence of steps for testing the registers was as follows:

1. Write "1" s into lower order bits of even registers.
2. Write "1 "s into upper order bits of odd registers.
3. Read (verify) "1 " s in upper order bits of odd registers, and write "0 "s into lower order bits of odd registers.
4. Read "1 " s in lower order bits of even registers, and write "0 "s into upper order bits of even register.
5. Read (00FF)* and write "0 "s over "1 " s in lower order bits of even registers.

NOTE: In defining a 16 bit pattern, four (4) hexadecimal characters are used.

6. Read (FF00) and write "0"s over "1"s in upper order bits of odd registers.

7. Read (0000) and write "1"s over "0"s in lower order bits of odd registers.

8. Read (0000) and write "1"s over "0"s in upper order bits of even registers.

9. Read (00FF), increment by 1, read (0100), write (3A52), read (3A52), and increment by 1 contents in register 1.

10. Read (FF00), increment by 1, read (FF01), write (4A53), read (4A53), and increment by 1 contents in register 2.

11. Read (00FF), increment by 1, read (0100), write (5A54), read (5A54), and increment by 1 contents in register 3.

12. Read (FF00), increment by 1, read (FF01), write (6A55), read (6A55), and increment by 1 contents in register 4.

13. The previous four steps are performed on the remaining 5 through 15 registers except a different pattern is written into each register.

14. Patterns remaining in registers after steps 9 - 13 are read from registers 1 through 15.

The sequence of operations performed by these tests on the scratch pad memory is summarized in Table 3-1. This table illustrates what test requirements were fulfilled.

Vendor E's tests did ensure that a 1 can be written over a 0 in the upper order bits of the even registers and the lower order bits of the odd registers. They also verified that a 0 can be written over a 1 in all the bit positions of the odd registers and the lower order bits of the even registers.

Writing a 1 over a 0 in all the lower order bits of the even registers and all the upper order bits of the odd registers, and writing a 0 over a 1 in all the upper order bits of the even registers was not verified.

Memory Cell Operation	Even Registers		Odd Registers		Capability Verified
Write		FF			
Write			FF		
Read			FF		
Write				00	
Read		FF			
Write	00	FF			
Write		00			Write 0 over 1 in E.0
Read			FF	00	
Write			00		Write 0 over 1 in 0.1
Read			00	00	
Write				FF	Write 1 over 0 in 0.0
Read	00	00			
Write	FF				Write 1 over 0 in E.1
Read	FF	00	00	FF	
Write & Read	FF	01	01	00	Write 0 over 1 in 0.0
Write & Read		Unique Patterns			
Write	Previous Pattern +1				
Read	Patterns in all registers after completing above sequence				

Table 3-1. Sequence of operations executed on scratch pad memory by Vendor E's tests.

Transmission gate bidirectional high impedance capability is ensured if prior to reading the data from a register under test its complemented data is read from or written into another register. Vendor E's patterns did not completely verify this capability in the scratch pad memory. A sample of registers investigated in detail showed that only one-fourth of the transmission gate high impedance states were tested with Vendor E's patterns.

SPM Test Development

The SPM tests received from Vendor E did not verify the operation of the SPM. No one requirement was completely checked with these tests. Since efforts to augment these patterns were very inefficient, a new set of tests were developed which verified the SPM. A cross reference of vector numbers to mnemonic instructions for the newly developed SPM test is listed in Table 3-2 (Sequence SP). Tektronix programs utilized in generating the test vectors are described in Appendix D.

Bit Independence and Integrity (Vectors 1-7424)

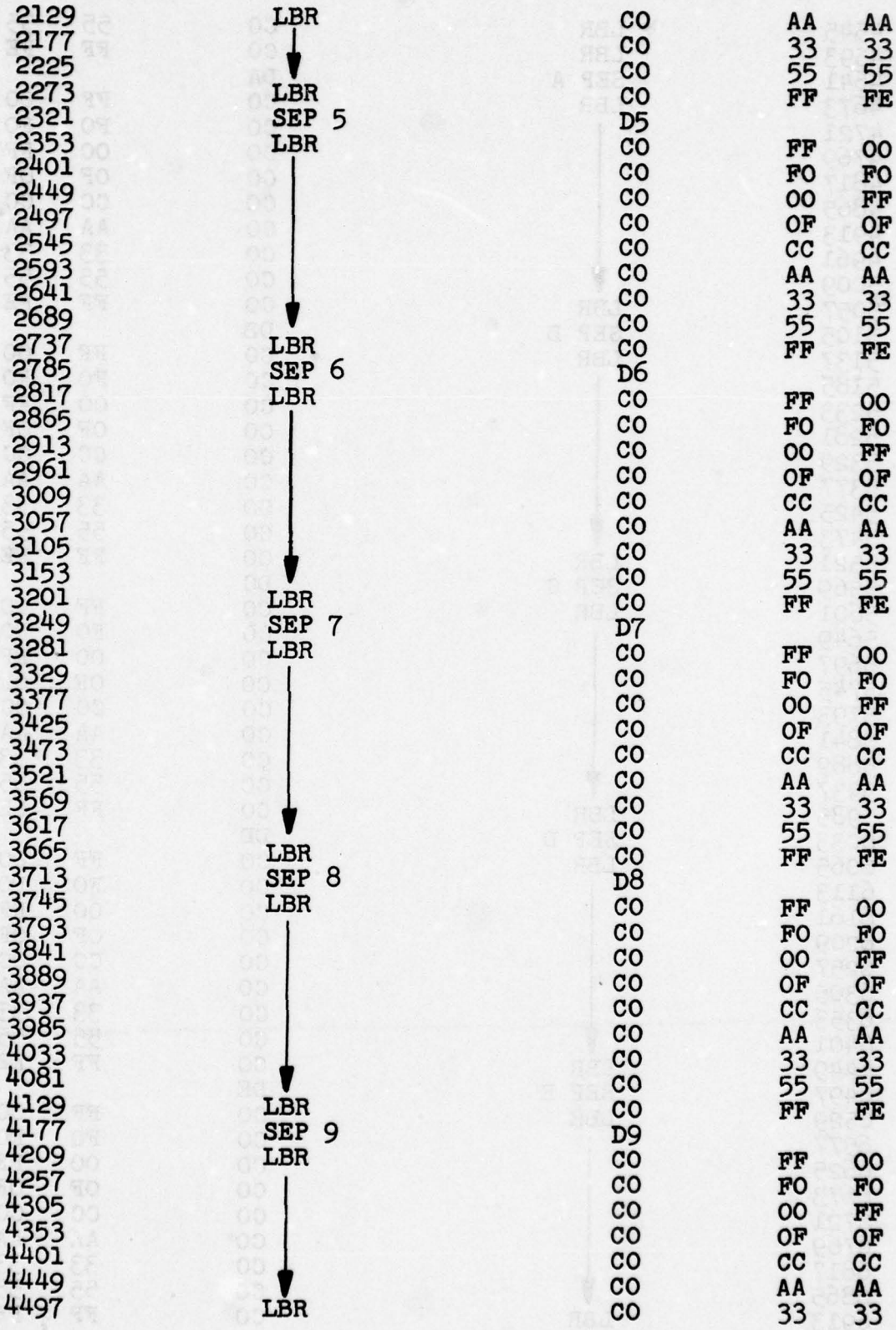
Bit independence in registers was verified by reading a 1 and a 0 in each bit position while the other bits contained the complemented state. The patterns developed consisted of writing 1's in the upper ordered 8 bits and 0's in the lower ordered 8 bits. This pattern and its complemented pattern show that the upper 8 bits and lower 8 bits are independent of each other. The next pattern consisted of alternating four 1's and four 0's in the registers. The succeeding pattern was its complement. After writing and reading these four patterns, isolation is verified between the first 4 bits and the remaining 12 bits, the second 4 bits and the 12 other bits, the third four bits and the 12 other bits, and the last 4 bits and the first 12 bits. This method was continued until alternating 1's and 0's were used and isolation between every bit was verified. Isolation, but not worst case leakage, between cells was checked with these patterns.

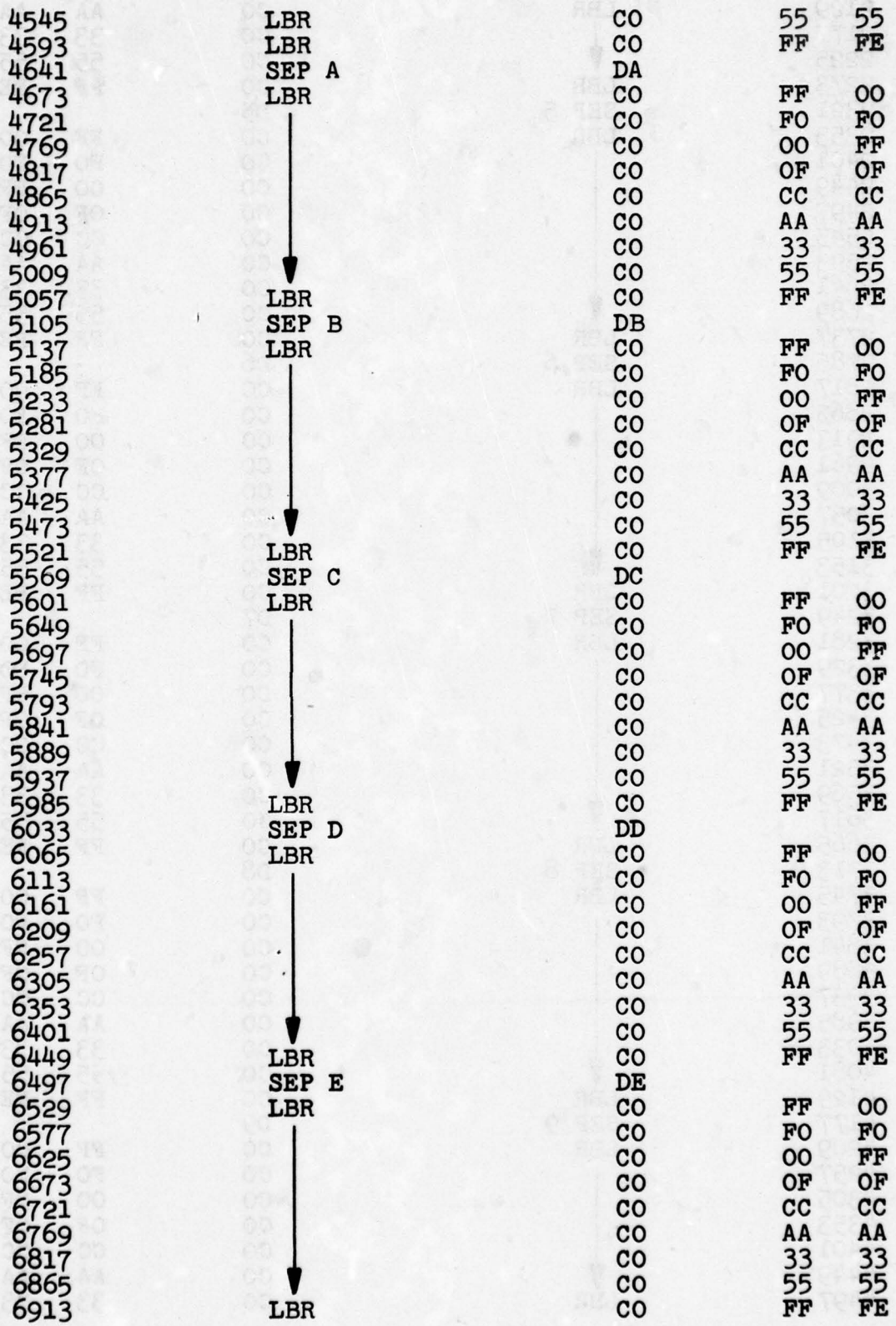
These patterns for verifying isolation were resequenced to ensure the capability of writing a 1 over a 0 and a 0 over a 1 in each bit (bit integrity). The resequenced patterns also verify the capability of writing a 1 over a 1 and a 0 over a 0. Vendor E's implementation of the SPM does not require this particular test (writing a 1 over a 1 and a 0 over a 0) since there are no feedback path connections. The resequenced patterns necessary to verify the above conditions are shown in Table 3-3.

OP Codes

Test No.	Mnemonic	Hexadecimal	Data
1	RESET & INITIALIZATION		
33	LBR	C0	FF 00
81		C0	F0 F0
129		C0	00 FF
177		C0	0F 0F
225		C0	CC CC
273		C0	AA AA
321		C0	33 33
369		C0	55 55
417	LBR	C0	FF FE
465	SEP 1	D1	
497	LBR	C0	FF 00
545		C0	F0 F0
593		C0	00 FF
641		C0	0F 0F
689		C0	CC CC
737		C0	AA AA
785		C0	33 33
833		C0	55 55
881	LBR	C0	FF FE
929	SEP 2	D2	
961	LBR	C0	FF 00
1009		C0	F0 F0
1057		C0	00 FF
1105		C0	0F 0F
1153		C0	CC CC
1201		C0	AA AA
1249		C0	33 33
1297		C0	55 55
1345	LBR	C0	FF FE
1393	SEP 3	D3	
1425	LBR	C0	FF 00
1473		C0	F0 F0
1521		C0	00 FF
1569		C0	0F 0F
1617		C0	CC CC
1665		C0	AA AA
1713		C0	33 33
1761		C0	55 55
1809	LBR	C0	FF FE
1857	SEP 4	D4	
1889	LBR	C0	FF 00
1937		C0	F0 F0
1985		C0	00 FF
2033		C0	0F 0F
2081	LBR	C0	CC CC

Table 3-2. Sequence SP - SPM test to OP code cross reference


2129 LBR C0 AA AA
2177 C0 33 33
2225 C0 55 55
2273 LBR C0 FF FE
2321 SEP 5 D5
2353 LBR C0 FF 00
2401 C0 F0 F0
2449 C0 00 FF
2497 C0 0F 0F
2545 C0 CC CC
2593 C0 AA AA
2641 C0 33 33
2689 C0 55 55
2737 LBR C0 FF FE
2785 SEP 6 D6
2817 LBR C0 FF 00
2865 C0 F0 F0
2913 C0 00 FF
2961 C0 0F 0F
3009 C0 CC CC
3057 C0 AA AA
3105 C0 33 33
3153 C0 55 55
3201 LBR C0 FF FE
3249 SEP 7 D7
3281 LBR C0 FF 00
3329 C0 F0 F0
3377 C0 00 FF
3425 C0 0F 0F
3473 C0 CC CC
3521 C0 AA AA
3569 C0 33 33
3617 C0 55 55
3665 LBR C0 FF FE
3713 SEP 8 D8
3745 LBR C0 FF 00
3793 C0 F0 F0
3841 C0 00 FF
3889 C0 0F 0F
3937 C0 CC CC
3985 C0 AA AA
4033 C0 33 33
4081 C0 55 55
4129 LBR C0 FF FE
4177 SEP 9 D9
4209 LBR C0 FF 00
4257 C0 F0 F0
4305 C0 00 FF
4353 C0 0F 0F
4401 C0 CC CC
4449 C0 AA AA
4497 LBR C0 33 33


4545 LBR CO 55 55
4593 LBR CO FF FE
4641 SEP A DA
4673 LBR CO FF 00
4721 CO F0 F0
4769 CO 00 FF
4817 CO 0F 0F
4865 CO CC CC
4913 CO AA AA
4961 CO 33 33
5009 CO 55 55
5057 LBR CO FF FE
5105 SEP B DB
5137 LBR CO FF 00
5185 CO F0 F0
5233 CO 00 FF
5281 CO 0F 0F
5329 CO CC CC
5377 CO AA AA
5425 CO 33 33
5473 CO 55 55
5521 LBR CO FF FE
5569 SEP C DC
5601 LBR CO FF 00
5649 CO F0 F0
5697 CO 00 FF
5745 CO 0F 0F
5793 CO CC CC
5841 CO AA AA
5889 CO 33 33
5937 CO 55 55
5985 LBR CO FF FE
6033 SEP D DD
6065 LBR CO FF 00
6113 CO F0 F0
6161 CO 00 FF
6209 CO 0F 0F
6257 CO CC CC
6305 CO AA AA
6353 CO 33 33
6401 CO 55 55
6449 LBR CO FF FE
6497 SEP E DE
6529 LBR CO FF 00
6577 CO F0 F0
6625 CO 00 FF
6673 CO 0F 0F
6721 CO CC CC
6769 CO AA AA
6817 CO 33 33
6865 CO 55 55
6913 LBR CO FF FE

```
6961  SEP F          DF
6993  LBR            C0          FF   00
7041                 C0          F0   F0
7089                 C0          00   FF
7137                 C0          0F   0F
7185                 C0          CC   CC
7233                 C0          AA   AA
7281                 C0          33   33
7329                 C0          55   55
7377  LBR            C0          FF   FF
7425  LDX            F0          00
7457  PLO 0          A0
7489  PHI 0          B0
7521  PLO 1          A1
7553  PHI 1          B1
7585  PLO 2          A2
7617  PHI 2          B2
7649  PLO 3          A3
7681  PHI 3          B3
7713  PLO 4          A4
7745  PHI 4          B4
7777  PLO 5          A5
7809  PHI 5          B5
7841  PLO 6          A6
7873  PHI 6          B6
7905  PLO 7          A7
7937  PHI 7          B7
7969  PLO F          AF
8001  PLO 8          A8
8033  PHI 8          B8
8065  PLO 9          A9
8097  PHI 9          B9
8129  PLO A          AA
8161  PHI A          BA
8193  PLO B          AB
8225  PHI B          BB
8257  PLO C          AC
8289  PHI C          BC
8321  PLO D          AD
8353  PHI D          BD
8385  PLO E          AE
8417  PHI E          BE
8449  LDX            F0          FF
8481  LBR            C0          FF   F0
8529  PLO 0          A0
8561  PHI 0          B0
8593  PLO 1          A1
8625  PHI 1          B1
8657  PLO 2          A2
8689  PHI 2          B2
8721  PLO 3          A3
8753  PHI 3          B3
```

```
8785    PLO 4           A4
8817    PHI 4           B4
8849    PLO 5           A5
8881    PHI 5           B5
8913    PLO 6           A6
8945    PHI 6           B6
8977    PLO 7           A7
9009    PHI 7           B7
9041    LBR             C0          FF   F0
9089    PLO 8           A8
9121    PHI 8           B8
9153    PLO 9           A9
9185    PHI 9           B9
9217    PLO A           AA
9249    PHI A           BA
9281    PLO B           AB
9313    PHI B           BB
9345    PLO C           AC
9377    PHI C           BC
9409    PLO D           AD
9441    PHI D           BD
9473    PLO E           AE
9505    PHI E           BE
9537    SEP 0           D0
9569    LDX             F0          00
9601    LBR             C0          0000
9649    PHI F           BF
9681    PLO F           AF
9713    PHI E           BE
9745    PLO E           AE
9777    PHI D           BD
9809    PLO D           AD
9841    PHI C           BC
9873    PLO C           AC
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9937    PLO B           AB
9969    PHI A           BA
10001   PLO A           AA
10033   PHI 9           B9
10065   PLO 9           A9
10097   PHI 8           B8
10129   PLO 8           A8
10161   PLO 0           A0
10193   PHI 7           B7
10225   PLO 7           A7
10257   PHI 6           B6
10289   PLO 6           A6
10321   PHI 5           B5
10353   PLO 5           A5
10385   PHI 4           B4
10417   PLO 4           A4
10449   PHI 3           B3
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10481   PLO 3           A3
10513   PHI 2           B2
10545   PLO 2           A2
10577   PHI 1           B1
10609   PLO 1           A1
10641   LDX             F0      FF
10673   LBR             C0      FF   F0
10721   PHI F           BF
10753   PLO F           AF
10785   PHI E           BE
10817   PLO E           AE
10849   PHI D           BD
10881   PLO D           AD
10913   PHI C           BC
10945   PLO C           AC
10977   PHI B           BB
11009   PLO B           AB
11041   PHI A           BA
11073   PLO A           AA
11105   PHI 9           B9
11137   PLO 9           A9
11169   PHI 8           B8
11201   PLO 8           A8
11233   LBR             C0      FF   F0
11281   PHI 7           B7
11313   PLO 7           A7
11345   PHI 6           B6
11377   PLO 6           A6
11409   PHI 5           B5
11441   PLO 5           A5
11473   PHI 4           B4
11505   PLO 4           A4
11537   PHI 3           B3
11569   PLO 3           A3
11601   PHI 2           B2
11633   PLO 2           A2
11665   PHI 1           B1
11697   PLO 1           A1
11729   SEP 1           D1
11761   LBR             C0      FEDC
11809   SEP 2           D2
11841   LBR             C0      89AB
11889   SEP 4           D4
11921   LBR             C0      76   54
11969   SEP 8           D8
12001   LBR             C0      0123
12049   SEP E           DE
12081   SEX E           EE
12113   STR 1           51
12145   SEX 1           E1
12177   INP E           6E      00
12209   SEP D           DD
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12241   SEX D       ED
12273   STR 2       52
12305   SEX 2       E2
12337   INP D       6D      00
12369   SEP B       DB
12401   SEX 4       E4
12433   INP B       6B      00
12465   SEX B       EB
12497   STR 4       54
12529   SEX 8       E8
12561   SEP 7       D7
12593   OUT 7       67      00
12625   SEX 7       E7
12657   STR 8       58
12689
```

1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
1	1	1	1	0	0	0	0	1	1	1	1	0	0	0	0
0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	0	0	0	0	1	1	1	1
1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1
0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1

Table 3-3. Test pattern sequence for verifying bit independence and integrity.

Register Independence and Transmission Gate Isolation (Vectors 7425-11728)

Operations on one register must not affect or be affected by any other register in the SPM register array. Independence between registers must be tested to ensure this condition.

Verification of register independence in the SPM was performed in two parts. The first part ensured that writing into lower ordered registers had no effect on any higher ordered register, and the second portion ensured that writing into higher ordered registers had no effect on any lower ordered registers.

Upon completion of verifying bit independence and integrity all the SPM registers are filled with 1's. These 1's are read out of the registers and 0's are written into them. This process of writing 0's over 1's is performed on the SPM in ascending register order starting with register 0 and continuing to register E, register F is used as the program counter register. These tests show that writing zeros in lower ordered registers has no effect on 1's in any higher ordered register. This process is repeated except 0's are read out of the SPM registers while writing 1's into them in the same ascending register order. At this point in the test sequence it has been shown that writing 0's or 1's into lower ordered registers has no effect on any higher ordered register.

The second part of verifying register independence in the SPM was performed using the same technique as the first part except the order of accessing the registers was reversed. That is the first register accessed was F, the last register accessed was 1, and register 0 was the program counter. Thus, showing that writing 0's or 1's into higher ordered registers has no effect on any lower ordered register.

In addition to showing register independence, these tests were used to verify TG isolation in each memory cell. Prior to reading a bit from a register under test its complement was written into the program counter register. Thus, if TG isolation was inadequate either the PC register or the register under test would produce wrong data on the MA outputs. The PC register was initially loaded with 0000_{16} when the sequence of reading 1's was performed in ascending register order and again loading 0000_{16} into the PC preceding this operation on registers 8 through F. The PC register was loaded with FFFO preceding the operation of reading 0's in ascending register order and again reloading FFFO into the PC register preceding this operation on registers 8 through F.

This preloading procedure verified TG isolation for 1, 0 and a 0, 1 condition in every register.

Verification of 4 to 16 Decoder Interconnections (Vectors 11729 - 12688)

One of three registers, designated by P, X, and N, selects any one of the 16 SPM registers. Connections from the decoder to the SPM cells were verified in the register independence tests on the SPM. The connections from each of the three designating registers to the 4 to 16 bit SPM decoder must also be ensured.

The technique used to ensure these decoder connections consisted of writing unique data into SPM registers 1, 2, 4, and 8 using designating register P. This unique data was read out of each SPM register by selecting it via designating register N while the complement of register N is in P and X. This is repeated for designating register X. The designating data 1 (0001), 2(0010), 4(0100), and 8(1000) also verifies independence of each data line and bit in the designating registers by walking a one through a field of zeros.

1802 Control Logic Test Development (Test Sequence CL)

Verification of the remaining circuitry was accomplished by separating it into specific functions and ensuring that each functional block was tested. These blocks consisted of timing circuitry, I and N decoders, arithmetic logic unit, I/O interrupt servicing logic, conditioning short/long branch/skip logic, SPM increment/decrement logic, and registers D,B,N,I,P,T, and X. Test requirements for each block were defined and the testing effectiveness of Vendor E's tests for each block was evaluated. Tests were inserted or appended where necessary. Vendor E's test patterns and GEOS's insertions comprise vectors 1-2754 of sequence CL. The remaining vectors 2755-5938 were appended to complete the testing of functional blocks with proven test patterns.

Table 3-4 contains a cross reference between vector numbers in sequence CL to OP codes and data. The two rows of register

data indicate the data verified (top data) and stored (bottom data) for each instruction. The table uses hexadecimal notation to represent 4 bits of binary data.

Test numbers refer to the start of the fetch cycle for the specified OP codes. As shown in this table only five of the SPM registers (registers 0,1,2,7 and F) are utilized extensively in this sequence. All SPM registers are thoroughly tested in sequence SP

The following sections describe the required tests for each function, and methods of implementing these tests in the microprocessor.

Timing Circuitry

The basic timing signals in the 1802 microprocessor are produced by two blocks of circuitry.

The first block, generation, generates pulses corresponding to specific clock cycles. The second block, decoding, provides desired pulses from the generated signals. The signals from this timing circuitry are gated with other control logic signals to produce the desired synchronous signals. The signals from the timing decoder circuitry occur every eight clock pulses (1 machine cycle). Every machine cycle is dependent on the occurrence of these basic timing signals. Therefore, applying inputs and monitoring outputs defined in worst case timing diagrams ensures the operation of the timing generation circuitry.

I and N Decoders and Register Control Logic

The I and N decoders translate the contents of the I and N registers (OP code) into signals required for the operation of the remaining control logic. The initial I decoder is a 4 to 16 bit decoder. To verify the operation of this circuitry all combinations of I must be applied, i.e., every instruction type must be executed. The N decoder is not a straight 4 to 16 bit decoder. It consists of control logic which does not require application of every combination of N to verify its operation.

The Register control logic consists of logic which directly controls the operation of the registers. Specific output combinations from the I and N decoders are gated with timing signals to control registers. The major portion of this logic is exercised during ALU operations ($I = 7_{16}$ or F_{16}).

The decoder and register control logic circuitry was verified by insuring that every gate was exercised with their proven test vectors. Signals to each gate were defined and input conditions analyzed to ensure that the gates were verified. The original control logic tests met the GEOS testing requirements for this portion of the control logic circuitry and no tests were added.

TEST NO.	MNEMONIC	HEXADECIMAL DATA														
		IN		P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
1	RESET	00		0	0				1	0						
5	INITIALIZE											0000				
23	DMA-OUT		00									0000 01				
39	LD2	02	00	0				00			6	0001 0002				
71	ADD	F4	CB	0			0	CB			B	0002 0003				
103	SEX 1	E1		0	1						0	0003 0004				
135	PLO 1	A1		0				CB			C	0004 0005	CB			
167	PHI 1	B1		0				CB			8	0005 0006	CB CB			
199	PLO 2	A2		0				CB			3	0006 0007		CB		
231	PHI 2	B2		0				CB			8	0007 0008		CB CB		
263	MARK	79		0	1 0	10					6	0008 0009		CBCB CBCA		
295	SAV	78		0		10					F	0009 000A				
327	LBNF	CB	00 09	0							F	000A 0009				
375	INP 9	69	8C	0				8C			0	0009 000A				
407	INTERRUPT			0 1	2	00			0		8	000A				
423	STXD	73		1				8C			F		CBCB CBCC	CBCA CBC9		
455	INC 1	11		1							0		CBCC CBCE			
487	SEQ	7B	CC	1						1	A		CBCE CBCF			

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL IN	DATA	P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
519	REQ	7A		1						0	0		CBCF CBD0			
551	SKP	38	CC	1							1		CBD0 CBD2			
583	BQ	31	56	1							3		CBD2 CBD4			
615	B1	34	13	1							2		CBD4 CBD6			
647	BNZ	3A	28	1							6		CBD6 CB28			
679	SEX 0	E0		1	0						6	000A	CB28 CB29			
711	LDA 0	40	00	1				00			6	000A 000B	CB29 CB2A			
743	SMI	FF	01	1			0	FF			6		CB2A CB2C			
775	STR 0	50		1				FF			6	000B	CB2C CB2D			
807	IDL	00	40 3A	1							6	000B 000C	CB2D CB2E			
855	DMA-IN		01 10								6	000C 000D				
887	OUT 5	65	30	1							2	000D 000E	CB2E CB2F			
919	DEC 2	22		1							6		CB2F CB30	CBC9 CBC8		
951	GLO 0	80		1				OE			6	OE	CB30 CB31			
983	PLO 7	A7		1							6		CB31 CB32		OE	
1015	GHI 2	92		1				CB			6		CB32 CB33	CBC8		
1047	PHI 7	B7		1				CB			6		CB33 CB34		CB	

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL IN	DATA	P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
				1				≠00					CB34			
1079	LSNZ	C6	04 6A								A		CB37			
				1	0	00						000E	CB37			
1127	SAV	78									E		CB38			
				1	0							000E	CB38			
1159	LDXA	72	75					75			2	000F	CB39			
				1	0							000F	CB39			
1191	STXD	73									8	000E	CB3A			
				1					0				CB3A			
1223	LSIE	CC	77 EE								3		CB3B			
				1	0							000E	CB3B			
1271	RET	70	10	0	1				1		4	000F	CB3C			
				0					1			000F				
1303	LSIE	CC	73 AB								0	0012				
				0	1							0012	CB3C			
1351	DIS	71	01	1	0				0		8	0013	CB3D			
				1					0				CB3D			
1383	LSIE	CC	00 00								F		CB3E			
				1			0						CB3E			
1431	BDF	33	00								F		CB40			
				1	0							0013	CB40			
1463	ADC	74	18				0	8D			3		CB41			
				1												
1486	WAIT (6)															
1498	WAIT (15)															
				1			0						CB41			
1517	BNF	3B	FE								0		CBFE			
				1									CBFE			
1549	SHLC	7E					1	1A			0		CBFF			
								1A					CBFF			
1583	PHI 1	B1									0		1A00			
				1									1A0C	CBC8		
1615	SEP 2	D2		2							B		1A01			
				2										CBC8		
1647	SHR	F6					0	0D			E			CBC9		

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL IN	DATA	P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
				2							1			CBC9		
1679	B1	34	9F											CB9F		
				2										CB9F		
1711	OR	F1	55					5D			0			CBA0		
				2				5D						CBA0	CB0E	
1743	PLO 7	A7									3			CBA1	5D	
				2							2			CBA1		
1775	B2	35	30											CB30		
				2	0							0013		CB30		
1807	AND	F2	66					44			A			CB31		
				2							4			CB31		
1839	B3	36	FE											CBFE		
				2										CBFE		
1871	XRI	FB	AA					EE			E			CC00		
				2				EE						CC00	CB5D	
1903	PHI 7	B7									0			CC01	EE	
				2							8			CC01		
1935	B4	37	00											CC00		
				2	0							0013		CC00		
1967	SD	F5	FF			1		11			F			CC01		
				2				11				0013		CC01		
1999	PLO 0	A0									7	11		CC02		
				2	0							0011		CC02		
2031	SMB	77	FE			0		13			0			CC03		
				2		0								CC03		
2063	LSDF	CF	12 34								A			CC04		
				2					13			00		CC04		
2111	PHI 0	B0									A	13		CC05		
2128	WAIT (1)															
				2								1311				
2129	LOAD											1312				
2176	DMA-IN		34 85													
2219	WAIT (1)															

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL IN	DATA	P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
				2								1313		CC05		
2225	RET	70	10	0	1				1			1314		CC06		
												1314				
2257	DMA-IN											1315				
												1315				
2273	INTERRUPT		54	1	2	10			0							
				1	2	10							1A01	CC06		
2289	SAV	78											1A02			
				1								1315				
2321	DMA-OUT		47									1316				
				1								1316				
2340	RESET			0	0				1	0						
				0												
2341	INITIALIZATION											0000				
				0								0000				
2359	DMA-IN		33									0001				
2375	LOAD															
				0								0001				
2397	DMA-OUT		58									0002				
				0								0002	1A02			
2413	SEX 1	E1			1							0003				
2435	WAIT (1)															
				0												
2437	LOAD															
				0												
2465	INTERRUPT			1	2	10			0							
2481	IDL		10	1												
											8					
				1								0003				
2515	DMA-IN											0004				
				1									1A1B	CC06		
2531	RET	70	07	7	0				1		0		1A1C	CC07		

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL DATA IN		P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
				7								0004				
2563	DMA-IN		EF								0	0005				
				7											EE5D	
2579	ADCI	7C	2A				0	3D			0				EE5F	
				7								0005				
2611	DMA-IN										0	0006				
				7				3D							EE5F	
2627	STR 7	57									F				EE60	
				7			0								EE60	
2659	LBNF	CB	CC 07								F				CC07	
				7						0					CC07	
2707	LBNQ	C9	44 31								F				4431	
				7											4431	
2755	SEQ	7B	AB							1	F				4432	
				7	0							0006			4432	
2787	RET	70	12	2	1				1		F	0007			4433	
				2	1								1A1C	CC07		
2819	LDX	F0	00					00			F			CC08		
				2									1A1C	CC08		
2851	SD	F5	00				1				F			CC09		
				2							7			CC09		
2883	B4	37	DE											CC0B		
				2							B			CC0B		
2915	B3	36	E7											CC0D		
				2							D			CC0D		
2947	B2	35	CE											CC0F		
				2							E			CC0F		
2979	BN1	3C	FF											CCFF		
				2	1								1A1C	CCFF		
3011	DIS	71	21	1	2				0		F		1A1D	CD00		
				1									1A1D			
3043	NOP	C4	00 00								F		1A1E			
				1									1A1E			
3091	NBR	38	00								F		1A20			

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL IN	DATA	P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
				1					0				1A20			
3123	LSIE	CC	0000								F		1A21			
				1									1A21			
3171	ADI	FC	00				0	00			F		1A23			
				1	2								1A23	CD00		
3203	RET	70	12	2	1				1		F		1A24	CD01		
				2			0							CD01		
3235	BDF	33	FF								F			CD03		
				2	1								1A24	CD03		
3267	SD	F5	40				1	40			F			CD04		
				2				≠00						CD04		
3299	BZ	32	FF								F			CD06		
				2										CD06		
3331	SMBI	7F	20				1	20			F			CD08		
				2				≠00						CD08		
3363	BNZ	3A	FF								F			CDFF		
				2	1								1A24	CDFF		
3395	SM	F7	10				1	10			F			CE00		
				2				≠00						CE00		
3427	LBZ	C2	00 00								F			CE03		
				2	1								1A24	CE03		
3475	XOR	F3	18					08			F			CE04		
				2				08					1A24	CE04		
3507	STXD	73									F		1A23	CE05		
				2				≠00						CE05		
3539	LSNZ	C6	0000								F			CE08		
				2										CE08		
3587	SDBI	7D	0C				1	04			F			CE0A		
				2				≠00						CE0A		
3619	LBNZ	CA	07FF								F			07FF		
				2										07FF		
3667	SDI	FD	06					02			F			0801		
				2				≠00						0801		
3699	LSZ	CE	FFFF								F			0802		

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL IN	DATA	P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
				2										0802		
3747	LDI	F8	80					80			F			0804		
				2	1			80					1A23	0804		
3779	STXD	73									F		1A22	0805		
				2				≠00						0805		
3811	BZ	32	FF								F			0807		
				2										0807		
3843	SHLC	7E	00				1	01			F			0808		
				2				≠00						0808		
3875	BNZ	3A	FF								F			08FF		
				2	1								1A22	08FF		
3907	DIS	71	07	7	0				0		F		1A23	0900		
				7											4433	
3939	SMBI	7F	02				0	FF			F				4435	
				7						1					4435	
3971	LSNQ	C5	FFFF								0				4436	
				7											4436	
4019	REQ	7A	00							0	F				4437	
				7											4437	
4051	ANI	FA	00					00			F				4439	
				7				=00							4439	
4083	BNZ	3A	FF								0				443B	
				7								0007			443B	
4115	SD	F5	FF				1	FF			F				443C	
				7			1								443C	
4147	LBDF	C3	4F FF								0				4FFF	
				7	0							0007			4FFF	
4195	RET	70	FF	F	F				1		0	0008			5000	
				F												FFFE
4227	LBR	C0	FFFE								F					
				F	F	10								0900		FFFE
4275	MARK	79			F	FF					F			08FF		FFFF
				F								0008				FFFF
4307	GHI 0	90						00			F					0000

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL IN	DATA	P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
				F												0000
4339	LBR	C0	7FFF								F					7FFF
																7FFF
4387	STXD	73		F	F			00			F					8000
				F										08FF		7FFF
4419	GLO 2	82						FF			F					8000
				F												8000
4451	LBR	C0	3F FF								F					3FFF
																3FFF
4499	STXD	73		F	F			FF			F					4000
				F												3FFF
4531	LBR	C0	1FFF								F					1FFF
				F												1FFF
4579	DEC F	2F									F					2000
				F												1FFF
4611	LBR	C0	0FFF								F					0FFF
																0FFF
4659	STXD	73		F				FF			F					1000
				F												0FFF
4691	LBR	C0	F7FF								F					F7FF
				F												F7FF
4739	DEC F	2F	99								F					F800
				F												F7FF
4771	LBR	C0	E3FF								F					E3FF
																E3FF
4819	DEC F	2F	AA	F							F					E400
				F												E3FF
4851	LBR	C0	D1FF								F					D1FF
																D1FF
4899	STXD	73		F	F			FF			F					D200
				F	F											D1FF
4931	OUT 1	61	AA								F					D2FF
				F	F											D201
4963	OUT 2	62	AA								F					D203

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL IN	DATA	P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
				F	F											D203
4995	OUT 4	64	AA								F					D205
				F												D205
5027	SEX F	EF			F						F					D206
				F												D206
5059	SEP 0			0							F					D207
				0	F	FF						0008		08FF		
5091	MARK	79			0	FO					F	0009		08FE		
				0								0009				
5123	SEX C	EC			C						F	000A				
				0								000A				
5155	SEP C	DC		C							F	000B				
				C	C	FO								08FE		
5187	MARK	79			C	CC					F			08FD		
				C								000B				
5219	SEX 0	EO			0						F					
				C												D207
5251	SEP F	DF		F							F					
				F	0	CC								08FD		D207
5283	MARK	79			F	OF					F			08FC		D208
				F												D208
5315	SEX 3	E3			3						F					D209
				F												D209
5347	SEP 3	D3		3							F					D20A
				3	3	OF								08FC		
5379	MARK	79			3	33					F			08FB		
				3												
5411	SEX A	EA			A						F					
				3												
5443	SEP A	DA		A							F					
				A	A	33										
5475	MARK	79			A	AA					F			08FB		
				A										08FA		
5507	SEX 5	E5			5						F					

Table 3-4. Register definition for test sequence CL.

TEST NO.	MNEMONIC	HEXADECIMAL IN	DATA	P	X	T	DF	D	IE	Q	EF	R(0)	R(1)	R(2)	R(7)	R(F)
				A												
5539	SEP 5	D5		5							F					
				5	5	AA								08FA		
5571	MARK	79			5	55					F			08F9		
5603	DIS	71	07	7	0				0		0					
							1								5000	
5635	LSDF	CF	ABCD								0				5003	
												000B			5003	
5683	SDB	75	55				0	56			0				5004	
												000B			5004	
5715	AND	F2	A9					00			0				5005	
								00							5005	
5747	LSZ	CE	4321								0				5008	
															5008	
5795	SEQ	7B								1	0				5009	
															5009	
5827	LDA	47	55					55			0				500B	
										1					500B	
5859	LSQ	CD	5678								0				500E	
								55							500E	D20A
5907	STR	5F	00								0				500F	

Table 3-4. Register definition for test sequence CL.

Arithmetic Logic Unit (ALU)

The ALU in the 1802 microprocessor operates on one bit of data at a time. Operand data is serially shifted from the D and B (transparent to the user) registers. The output of the ALU is shifted back into the D register. When an ALU operation is performed, the ALU executes the function eight times, once on each pair of bits in the D and B registers. One ALU operation applies eight patterns of data to the ALU.

The vectors applied to the ALU by Vendor E's tests were evaluated using a computer program to determine their TCL. Vendor E's tests obtained a TCL of 96.6%. The program generated two more vectors and a third was manually generated to obtain a TCL of 100%.

The vectors which the program generated consisted of executing a load operation of a 0 (read from memory) into a bit position which was a 1 (contents of D register) and the other consisted of exclusive ORing a 1 with a 1. The manually generated vector consisted of subtracting a 1 in the D register from a 0 in the memory. These three vectors were applied to the ALU in the patterns appended to the control logic tests (Tests 3267, 3475, and 3747).

I/O Interrupt Servicing

The circuitry involved in servicing interrupts utilizes latches which are strobed during execution cycles. The priority of servicing these interrupts is also included in this circuitry. This section of the processor was analyzed using the same method used to evaluate the vectors for the register control logic.

Vendor E's tests acknowledged all three I/O requests and ensured that each request was serviced. All priorities were verified by these tests.

Conditional Short/Long Branch/Skip

The circuitry involved in conditional short/long branches/skips consists of multiplexers and gated control logic. A condensed drawing of this circuitry is shown in Figure 3-3. The flagged states are selected by bits 0 - 2 from the N register and gated with signals from the timing and I decoders. The test philosophy for multiplexers is to ensure that each channel can transfer both a logic "1" and "0" independent of the other channels. The gate level analysis of this circuitry also showed that every flagged state must be tested when all other flags are in the opposite state.

Vendor E's tests executed a check on every flag, but not both states of every flag were used nor were the other flags in the appropriate states for a thorough test. These tests were

revised if the flag states were easily changed such as $\overline{EF}$ inputs. Otherwise, additional tests were added to verify untested conditions (vectors 2755 - 4195 and 5603 - 5938 in sequence CL).

One flag condition which required executing a given test condition more than once was for D $\neq$ 0. The 8 bits in the D register are OR ed together and this signal is multiplexed as a flag input as illustrated in Figure 3-3. Due to the OR function, a logic "1" must be walked through zeros in the D register and this condition (D $\neq$ 0) tested for each bit to ensure this circuit operation.

The $\overline{IE}$ flag signal is gated with N3 and N2 which provides a signal defined by $\overline{N3 + IE + N2}$. Thus, to verify this circuitry a logic "0" must be walked through a field of logic "1"s for signals N3, N2, and $\overline{IE}$. Hexadecimal OP codes which test this circuitry and sensitize a path to an observable output are CC (Long skip if IE) with IE = 0 and 1, 38 (Never Branch) or C8 (Never long branch) with IE = 0 and C4 (No Operation) with IE = 0. Tests were appended to Vendor E's vectors for detecting these path sensitivities (Tests 3043 - 3170).

SPM Increment/Decrement Addresses

The increment and decrement functions on the memory addresses are performed in parallel on the 8 lower then 8 higher ordered bits. A separate distinct block executes these functions on the memory addresses as illustrated in Figure 3-4. The gate level schematics of the increment/decrement circuitry were investigated. In spite of the fact that even and odd bits utilize a different gate implementation for increment and decrementing both are verified with the same set of vectors.

When both the increment and decrement operation detected identical faults, the incrementing test pattern was selected since most instructions use this operation. The minimum tests required to verify the increment/decrement circuitry consisted of incrementing each bit with every combination of the carry-in bit (from the lower significant bit) and SPM bit, and decrementing each bit with the carry-in bit set and a 1 and 0 condition in the SPM bit. Since the upper ordered eight bits use the same increment/decrement circuitry as the lower ordered eight bits only the upper bits were utilized. Vendor E's vectors did not perform extensive testing on this increment/decrement circuitry. Therefore, vectors 4227 - 4899 in sequence CL were added to properly test this circuitry.

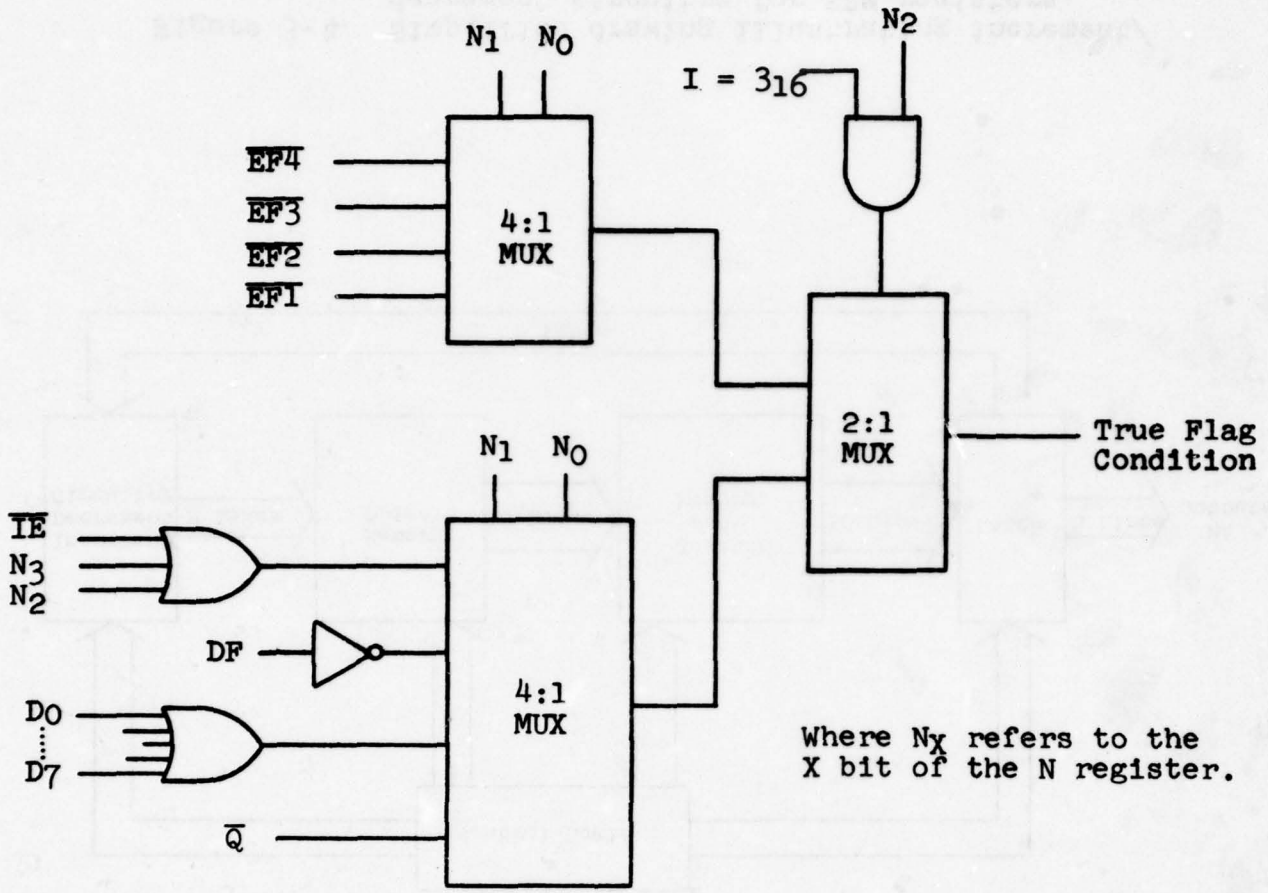


Figure 3-3 . Flag selection circuitry.

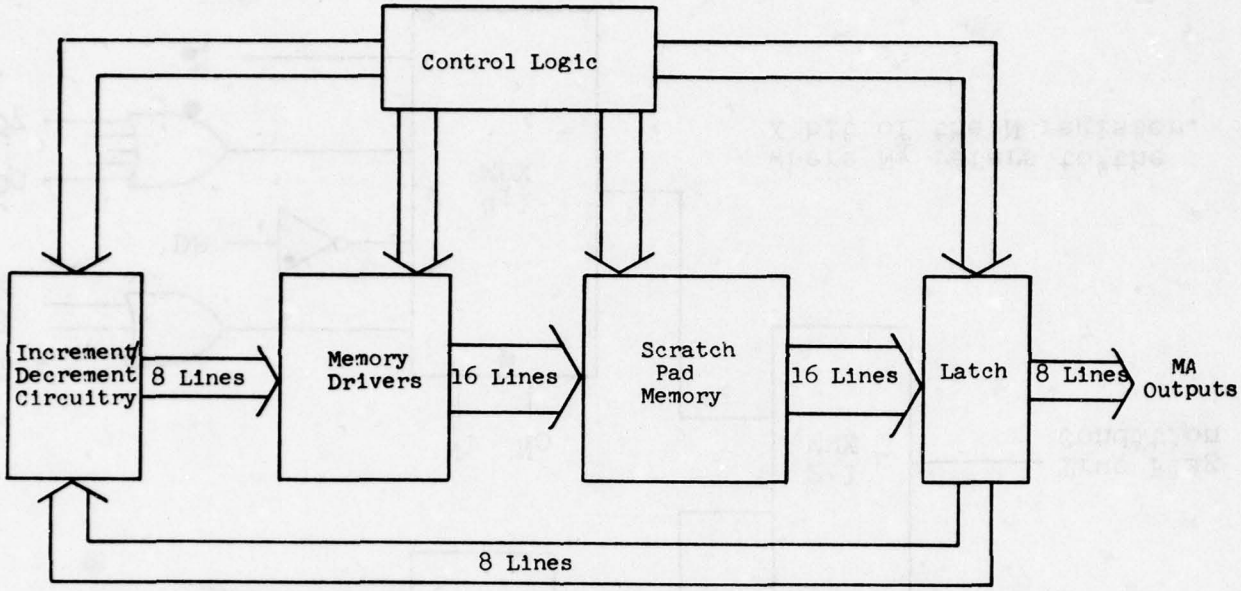


Figure 3-4. Simplified drawing illustrating increment/ decrement circuitry for SPM registers.

Registers (D, B, N, I, P, T, and X)

An operational description of these registers, with the exception of the B register, is given in Vendor E's 1802 device specification. The B register is not defined in their data sheet since its operation is transparent to the user. The B register is used to latch data from the BUS lines and is provided access to the D register through ALU operations.

Latch storage capability, TG isolation and transmitting capability, and data paths must be verified. During one ALU operation eight bits of data are shifted through both the D and B latches. These operations ensure latch storage capability, TG isolation and data paths. TG data transmitting capability for BUS lines to B and D registers is ensured during the SPM tests.

The P register designates the program counter register in the SPM. The data connnections, transmitting ability, and isolation from the BUS to the P register, and P register to the SPM address decoder were ensured during the SPM tests. The operation of the remaining latches and TGs were verified during the control logic tests, in particular data paths from the P to the T register are proven in the tests which were added to ensure the T register operation.

Vendor E's tests wrote and read hexadecimal numbers 10 and 00 into the T register. These patterns accomplished little in the area of ensuring the T register operation. Tests were added (vectors 5027 - 5602) which wrote and read, similar patterns used to verify bit independence in the SPM registers, into the T register. These patterns ensured register bit independence in addition to verifying that both a logic "1" and "0" could be written over a logic "0" and "1" respectively.

Verification of bit independence in the T register also ensured bit independence in the X register in addition to data paths between the X and T registers. TG isolation, bit independence, integrity, and data paths from the X register to SPM address decoder were verified in the SPM test, sequence SP table II (vectors 11729 - 12688). A logic 1 was walked through 0's in the X register and after loading each set of data it was verified along with data paths. This was accomplished by using the X register to select a unique SPM register. Thus, operations and connections utilizing the X register were verified.

Control Circuitry for N Outputs

Control logic signals are gated with N register bits 0 - 2 to provide the N outputs for input and output instructions (OP code = 6N for $1 \leq N \leq F$). Logic operation and data path integrity and independence must be ensured to verify this circuitry. Tests were added (vectors 4931 - 5026) to test sequence CL to perform these tests on this circuitry.

Test Vector Generation for Maximum Execution Frequency at Two Different Supply Voltages

Timing conditions were not checked in Vendor E's test vectors. Inputs were applied without verification of setup or hold times. The application of the vectors was slow enough so that the output signals were settle at the end of each vector.

Worst case timing conditions were incorporated into the revised vectors. A computer program was written to revise the generated vectors to include pattern changes as a function of timing. Setup and hold times for inputs were verified by forcing the correct data only during the specified time period and forcing its complement at all other times. Propagation delay times had to be considered when applying the patterns at maximum frequency. Applying the vectors at maximum frequency did not allow enough time for the outputs to settle before the application of the next vector. Fig. 3-3 and 3-4 illustrate the timing considerations used in generating maximum frequency test vectors. If an output was compared any time during a vector an L or H is specified in the vector, otherwise, an unknown condition was specified. The specified input data is included in vectors where the setup or hold times require the specified data to be present at least a portion of the vector time. Extra columns were added to the patterns to identify when the specified data on defined inputs should be applied per given timing waveforms, when a high ordered address is present at the MA outputs, and when the data bus is in the high impedance state.

Because propagation delay times for output signals overlapped into the next switching time period, it was necessary to specify a minimum propagation time for some waveforms. An example of this condition is the TPA output operating at a clock frequency of 3.47 MHz and $V_{DD} = V_{CC} = 10V$. The propagation delay times for this output are 300 ns maximum. As illustrated in Figure 3-5, falling clock edge number 1 forces output TPA to a logic 1. This level change may occur anytime within 300 ns after this clock edge. This propagation delay time period includes 12 ns of time after falling clock edge 2. Falling clock edge 2 forces the TPA output to a logic 0. So, theoretically if the propagation delay time of the low to high transition was maximum and the high to low delay was less than 12 ns, no high level

would occur on this output. Since all signals require time to propagate through the internal logic to an output, a minimum time was defined for the low to high propagation delay time. This minimum delay parameter was defined for signals TPA, TPB, and high ordered MA when $V_{CC} = V_{DD} = 10V$ and high ordered MA when $V_{CC} = V_{DD} = 5V$.

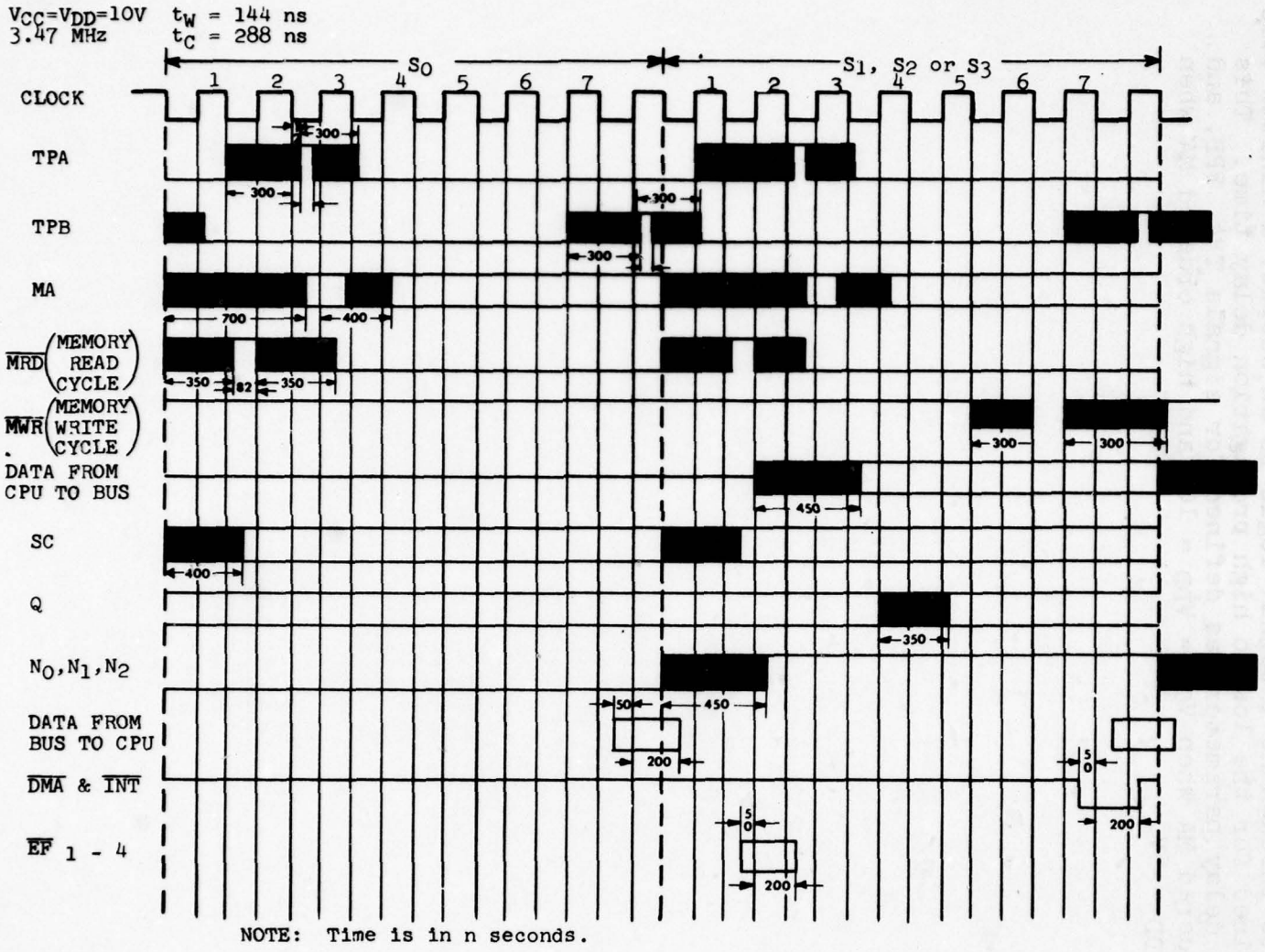
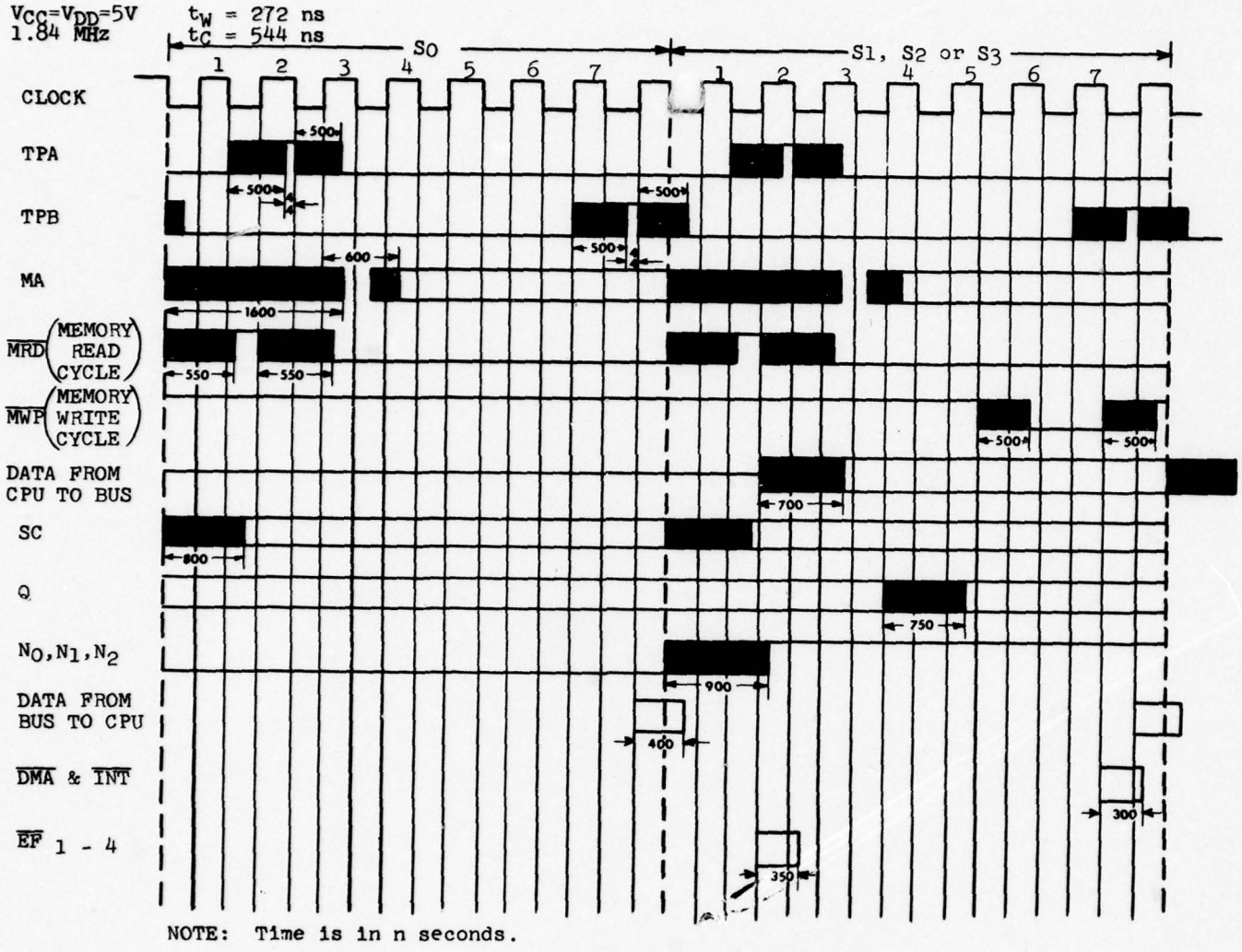


Figure 3-5. Worst case timing diagram for clock frequency of 3.47 MHz and $V_{CC} = V_{DD} = 10V$.



NOTE: Time is in n seconds.

Figure 3-6. Worst case timing diagram for clock frequency of 1.84 MHz and $V_{CC} = V_{DD} = 5V$.

SECTION IV

A COMPARISON OF TWO TEST PATTERNS DEVELOPED FOR THE CDP 1802 MICROPROCESSOR

The following is a review of the test vectors developed by Vendor H and Vendor J for NASA on the 1802 CMOS microprocessor. The review was made by comparing this pattern to that developed at GEOS for RADC for MIL-M-38510/470. Review of the patterns developed by Vendors H and J consisted of examining a report written for NASA entitled "An Electrical Characterization of the 1802 Microprocessor", investigating some specific patterns in detail, and discussing information requiring more in-depth knowledge of the instruction sequence with Vendor H.

The initial concern in reviewing these tests is the large number of vectors required to verify operation of the 1802 microprocessor. The main functional test developed for the NASA characterization consists of 11,818 vectors, where each vector is one complete clock cycle for the processor. The functional tests developed at GEOS consists of 18,290 vectors, where each vector is half a clock cycle. These would be reduced to half the number (9,146 vectors) if they were in the same form as NASA's vectors. The major difference in the number of vectors appears to be in the test development philosophies. Vendor J's test philosophy was based on testing a universal implementation of each of the processor's functions, whereas the test philosophy at GEOS was based on the exact logic implementation. This latter philosophy was followed since the two other sources for the 1802, Vendors K and H, have mask agreements with Vendor E. The development of the NASA vectors was also the result of reducing a 40,000 vector pattern to 11,818 vectors which may also explain the resultant difference in number of vectors.

A major portion of both patterns was devoted to verifying operation of the scratch pad memory (SPM) in the 1802 microprocessor. The test philosophy at GEOS for checking the SPM consisted of verifying bit and register independence (isolation) and integrity for both 1-0 and 0-1 conditions, transmission gate isolation capability, and data path integrity from designating registers N, P, and X to the SPM address decoder.

Since this was the philosophy followed at GEOS, all these conditions for the SPM are verified in the vectors developed at GEOS. The vectors reviewed in the NASA report do verify isolation in one direction but will not detect a diode type of short. For example, the patterns in sections 3.1.1 show that a 0 was written in bit 15 and a 1 was written in bit 7. This verifies isolation in one direction but will not detect a diode type of short where a 0 in bit 7 could pull down a logic 1 in bit 15. This condition was not checked on approximately 50% of the bits.

The procedure defined in paragraph 3.1.2 of the NASA report verifies the integrity (writing 1's over 0's and 0's over 1's) of every bit in the SPM. In addition to integrity, register independence is verified to a certain degree. The procedure described selects each register in turn and identifies it as a diagnostic register. 1's are written into it and the effect on the 0's stored in the other registers is checked. As other registers become the diagnostic register, previous diagnostic registers are periodically checked to see if the 0's now stored in them are being affected by the 1's being written in the new diagnostic register. The inverse of this pattern should also be applied, i.e.: the effect that writing 0's in the diagnostic register has on 1's stored in the other registers. The review of the patterns does not indicate that this was accomplished.

An investigation into the Vendor E implementation of the SPM showed that transmission gate (TG) isolation capability in the memory cells must be verified to ensure fault free operation (All memory cells in a specific bit position are connected to the same data line through TGs). To ensure TG isolation, prior to reading an SPM diagnostic bit, its complement should be read from another SPM register in the same bit location. This should be done for both the 0 and 1 conditions to thoroughly verify a TGs isolation capability. Independence and integrity of data paths from each of the designating registers, N, P, and X to the SPM address decoder must also be verified. Since determining the extent to which the NASA patterns accomplished the previous two tests would require a more detailed investigation, Vendor H was contacted. They indicated that these were not specifically tested for but that a good portion of the tests would be checked during the normal test pattern.

The test philosophy used by GEOS for the remaining circuitry consisted of separating the logic into specific functional blocks and verifying the circuitry in each block. The ALU circuitry operates on one bit of data each clock cycle and shifts the result back through the D register. Executing one ALU instruction will apply eight sets of data to the ALU. The sets of data applied to the ALU during the execution of the RADC vectors were evaluated by a computer program on the logic diagram for Vendor E's implementation. The evaluation indicated a 100% fault detection coverage by the data on the ALU, based on a stuck-at 1 and 0 philosophy. Time did not permit evaluating the NASA vectors which test the ALU. Since these patterns were generated to test all possible 1802 implementations, this portion of the test could yield a high testing confidence level for the ALU.

Both the NASA and RADC patterns verify that the proper priority is maintained during the application of DMA's and interrupt.

The branch and skip instructions are implemented in the 1802 by multiplexing the flagged states with the values of the instruction bits (N) used to select the correct flag. To thoroughly test a multiplexer requires verifying that each channel can pass both a one and zero independent of the other channels. This test philosophy is implemented by executing a conditional branch or skip instruction when each flag state is a 1 and 0 while the other flags are in the complemented state. Only the state of the external input flags ($\overline{EF1}$ - $\overline{EF4}$) were reviewed in the NASA vectors. These external input flags were in appropriate states to fulfill the necessary multiplexer tests during their conditional skips or branches. The states of the internal flags were not investigated during the execution of these instructions for this review, because it would require a significant amount of additional time. These must be investigated further to determine whether these multiplexer verification type of tests were completed. Vendor H indicated that the criteria of ensuring that the internal flag states were the complement of the tested conditional flag was probably not specifically tested.

The condition where D does not equal zero must be tested for each individual bit in the D register. This requires executing the conditional branch on D, with D not equal to zero, a minimum of eight times, once for each and only one bit equal to 1 in the D register. This condition was only executed five times and the data in the D register was not determined for this review.

Another functional block in the processor consists of the increment/decrement circuitry for the SPM registers. The Vendor E implementation uses an 8 bit increment/decrement circuit to operate on the 16 bit SPM registers. A 100% verification of stuck-at faults in this circuitry requires at a minimum incrementing and decrementing either all upper 8 bits, or lower 8 bits, or a correct combination of the two for both a one and zero condition with the carry bit equal to 1.

A 100% stuck-at fault detection would also require incrementing or decrementing a one and zero with the carry bit equal to zero. The patterns developed at GEOS execute these tests on the processor. The NASA vectors did not check the logic in this detail. To determine the extent of the circuitry verified would require a very detailed investigation of the SPM register contents.

The test philosophy at GEOS for verifying the operation of TGs consisted of transferring a 1 and 0 in both directions and assuring the isolation capability for a 1-0 and 0-1 condition. The capability of transferring data from the data bus to the SPM is verified during the tests on the SPM. The reverse transfer capability is performed only by the instructions GHI and GLO.

The NASA vectors did not pass both a 1 and 0 through these TGs in this direction. The vectors tested only 50% of this capability. During the execution of these instructions the data being transferred from the SPM to the D register is present on the data bus, but is not compared in the NASA vectors. This was also found to be the case for several instructions where the processor was supplying data to the data bus.

Verification of the T, X, and P registers for bit independence was assured completely in the NASA vectors by walking a 1 through each bit. During this verification the MARK instruction was executing repeatedly. Its execution continually transfers the contents of the T register to the data bus. The data bus contains the old contents of the T register during the earlier portion of the machine cycle and the new contents, loaded from the X and P register, later in the machine cycle. The vectors from NASA only test for the new contents of the T register on the data bus and no comparison for the old data is performed.

Independence and integrity of output lines N are verified by both sets of patterns. External input data is forced on the data bus only when it is being loaded into the processor in the NASA vectors. The vectors developed at GEOS force the complement of the data prior to and following the loading of the correct data. This ensures that the TGs connected to the data bus are isolating the registers at the correct times in the machine cycles.

If the NASA test pattern is revised to complete or add test sequences in the questionable areas that were discussed, the test confidence will be improved.

SECTION V

A COMPARISON OF TWO TEST PATTERNS DEVELOPED FOR THE 1802 CMOS MICROPROCESSOR

Introduction

GE OSPD and Vendor J both developed military specifications for the CDP 1802 Microprocessor. The major differences in the two specifications are in the test approaches utilized inverifying function, maximum frequency, threshold voltages, setup and hold times and propagation delay times. Advantages and disadvantages of these differences are discussed in the following report.

Comparison of Functional Tests

The functional tests developed by GE OSPD and Vendor J were developed separately to fulfill specific test philosophies. Therefore, distinct differences are present. Both functional test pattern files were generated utilizing computer programs which implies that either sequence could be converted to another format.

The most evident difference between the two pattern file formats is that one 1802 clock cycle requires one Vendor J vector versus two GE vectors. Since Vendor J uses one vector for each clock cycle the frequency resolution for applying the vectors with an automatic tester is better. In other words, application of the functional test closest to the maximum device frequency without exceeding it, is possible utilizing Vendor J's format (3.8 MHz) over GE's format (3.5 MHz).

The GE format defines the correct input data only when it is necessary to meet the setup and hold times. Otherwise the complement is denoted in the vectors. The Vendor J format defines the correct data on inputs also, but when data on the inputs is not critical the vectors inhibit tester drivers. Inhibiting the tester drivers leaves inputs floating. When the drivers are inhibited the charge on these pins cannot be drained quickly due to the low leakage of the MOS inputs in the 1802. Thus, data is maintained on the device inputs longer than indicated by the vectors, or required for a worst case test as it applies to set up and hold times. Internal timing will not be tested as thoroughly in the Vendor J vectors.

Vectors generated by GE also contain five additional columns of information. These define, when desired data is present in the vectors, when the high order address is available on the MA outputs, and when the data bus is in high impedance state. These additional columns are necessary for implementing the worst case timing conditions in the functional tests.

Functional tests are not performed at maximum frequency by Vendor J. But, since the 1802 propagation delays are somewhat long for specific signals, several clocks are applied at this intermediate frequency before output signals are settled and compared. Performing the functional tests at an intermediate frequency does not ensure worst case timing nor are specific responses to unique clocks verified. Worst case internal timing is only ensured by operating the device at its maximum frequency. If worst case internal timing is not being verified another method to check internal signals would be to compare the device outputs after every clock transition. This type of testing ensures the operation of gates which generate timing signals within the processor. A comparison of device outputs after every clock transition would require a reduction in clock frequency. This frequency would have to be reduced so that every output is settled and compared between each clock transition, thus, making the functional test look like more of a static test.

Test Philosophy Comparison

Conditions and verified parameters for each test philosophy in the 1802 microprocessor slash sheets are listed in Table 5-1. The leftmost column defines test type followed by GE OSPD's approach and then Vendor J's approach. Advantages and disadvantages of each approach are discussed with reference to the numbers in the rightmost column under comments.

Comments on Test Approaches

1. Test Pattern Development

   The GE philosophy of developing the functional tests using the actual vendor mechanization permits a reduction in the number of tests required to completely verify this device. Basing the functional tests upon a large functional block diagram as done by Vendor J requires more tests to completely verify each block. The effectiveness of this general approach should be immune to minor design changes which do not impact the functional blocks. But, design changes which affect output responses or timing would affect tests developed by both methods.

2. Input Signals

   Utilizing both logic 1 and logic 0 threshold voltages in functional testing as recommended by GE performs a more thorough verification of the device's thresholds and noise margins. At maximum frequency internal noise will be greater thereby increasing the opportunity for the device to fail

Test Type	GE Approach	Vendor J Approach	Comments
FUNCTIONAL TESTS	CONDITIONS:	CONDITIONS:	
	. Based on Actual Vendor Mechanization	. Based upon Large Functional Block Mechanization	1
	. Inputs are at Threshold	. Inputs not at Threshold	2
	. Outputs are Fully Loaded	. Outputs Capacitively Loaded (50 pf)	3
	. Test Patterns are Exercised at Maximum Frequency	. Test Patterns are Exercised at Some Frequency Significantly Less than the Maximum	4
	. Output Propagation Delays are Checked to Specified Limits	. Output Propagation Delays Not Checked at Specified Limits (Similar to Truth Table Test)	4
	. Worst Case Input Timing Conditions	. Input Timing Conditions Not at Worst Case Timing	4
DYNAMIC TESTS	. Completed during Functional. Test on a GO/NO-GO Basis and during Qualification Using Separate Test Pattern for Taking Variables Data	. Separate Test Patterns Specifically to Take Variables Data for: . Setup and Hold Times . Max. Frequency . Propagation Delays	5

Table 5-1. Slash sheet test outline

Test Type	GE Approach	Vendor J Approach	Comments
STATIC TESTS	PARAMETERS AND CONDITIONS:	PARAMETERS AND CONDITIONS:	
	. Capacitance (Variables Data and Testing Only During Qualification)	. Capacitance (Measured on all Devices)	6
	. Leakage	. Leakage	6
	. Input Clamp Characteristics	. Input Clamp Characteristics	6
	. Output Drive Levels . Logic "1"/"0" . High Impedance	. Output Drive Levels . Logic "1"/"0" . High Impedance	6
QUALIFICATION TESTS	. Capacitance . ZAP Test . Variables Data for Dynamic Tests	. ZAP Test	7

Table 5-1. Slash sheet test outline

if there are crosstalk and/or internal voltage biasing as a function of processing, layout, wiring and packaging. Since microprocessors are very complex, it is next to impossible to determine the worst case condition for any one input and sensitize it directly to an output. In the functional test more internal paths are exercised between more signals than in a separate test sequence which only activates specific data paths.

3. Output Loading

Fully loading outputs during the functional tests by OSPD performs a more thorough noise immunity check and more closely simulates system operation. Greater currents are switched, thereby giving the device an opportunity to generate more internal noise.

4. Maximum Frequency, Input and Output Worst Case Timing Conditions

Verifying worst case parameters during the performance of the functional tests as defined by GE OSPD ensures that all the internal timing of the microprocessor meets the specified requirements for all the instructions under worst case stimuli. Whereas the method used by Vendor J only verifies timing requirements along selected data paths through the microprocessor, because only selected instructions are executed at maximum frequency. Therefore, internal timing within the processor is not verified as well.

5. Dynamic Tests

These tests are performed to the specified limits on a GO/NO-GO basis during the functional test in the OSPD slash sheet. Variables data would be taken only for qualification testing utilizing separate test patterns. Vendor J records all the timing data for every device. This data is measured using separate test sequences. The separate patterns are repeated with one timing parameter tightened between passes until a failure occurs. When a failure occurs, the variable is recorded and this process repeated for the remaining variables. This measuring process increases test time considerably as compared to a GO/NO-GO type of test.

Since shorter pattern files are used for measuring the variables, only selected data paths are measured and may not be the worst case timing for each variable. Therefore, by performing these dynamic tests on a GO/NO-GO basis in the functional tests, worst case timing conditions will be detected that cannot be found in the separate shorter patterns. This would also reduce test time.

6. Static Tests

GE OSPD recommends measuring and recording capacitance data on a qualification basis only. Once the manufacturing process is defined and parts manufactured this parameter should not vary significantly. Vendor J recommends testing this parameter on all devices. This would significantly increase testing time and costs.

The philosophy of GE and Vendor J were in agreement for testing leakage currents, input clamping voltages, and output drive capability.

Vendor J measures the input threshold voltages by using a separate shorter pattern than the functional tests. This test only verifies the thresholds of selected input gates and may never sensitize them to an output as they would be during the functional tests.

7. Qualification Tests

Performing the high voltage (V_{Zap}) test as a qualification test was recommended by both GE OSPD and Vendor J since this is very difficult to perform and is demonstrating a maximum stress capability.

As denoted earlier GE OSPD recommends measuring and recording capacitance and dynamic parameters on a qualification basis only. The dynamic parameters would be verified on every device on a GO/NO-GO basis in the functional test i.e., no specific data would be measured.

Summary

Implementation of the functional tests as defined by GE OSPD may be more difficult than Vendor J's approach. But, once implemented the resulting test will be more thorough and test time significantly less. Marginal microprocessors will be readily screened during testing. Thus, eliminating devices that could be troublesome in systems designed close to the limits of the microprocessor.

It may be possible to implement the GE functional test to verify every worst case parameter in one pass due to tester differences. Variations in tester capabilities would require variations in the pattern files to perform worst case testing. But, once implemented, the dynamic functional test will perform a better check on the devices' parameters than if separate shorter patterns were utilized.

SECTION VI

DEVELOPMENT OF A LOGIC INTEGRITY TEST FOR THE 8228/8238, SCHOTTKY BIPOLAR, SYSTEM CONTROLLER AND BUS DRIVER FOR 8080A CPU

Objective

Develop a Logic Integrity Test (LIT) for the 8228/38, Schottky Bipolar System Controller and Bus Driver for the 8080A CPU.

Circuit Description

The 8228/38 consists of a bi-directional bus driver, status latch and gating array as shown in Figure 6-1. Figures 6-2 and 6-3 show Vendor A's and Vendor C's logic diagrams, respectively.

The bi-directional bus, which is eight bits wide, provides isolation of the CPU data bus from the system data bus. A high on DBIN enables the CPU data bus and a low places it in the high impedance state. The system data bus is enabled and disabled by a 3 input OR gate (G1). The inputs to this gate are STSTB, $\overline{\text{BUSEN}}$ and $\overline{\text{WO}}$. All of the inputs to this gate must be low to enable the system data bus, while any high input will disable it.

The status latch is a combination of 6 flip-flops and various gates. The flip-flops are D-type; that is, when the clock inputs are high data is transferred directly to the outputs and when the clock is low the outputs remain in the previous state independent of the D inputs.

The gating array, which generates the control outputs, is strictly combinational logic with tri-state outputs. All of the outputs are enabled when $\overline{\text{BUSEN}}$ is low and disabled when it is high. The $\overline{\text{INTA}}$ control signal is normally used to gate the "interrupt instruction port" onto the bus. However, if the $\overline{\text{INTA}}$ output is tied to a +12V supply through a series 1K ohm resistor, the device will automatically insert a RST7 instruction onto the bus at the proper time. This is useful in small systems where only one basic vector is needed in the interrupt structure.

The difference between the 8228 and 8238 is shown in the upper right corner of Figure 6-2. The 8228 has no connection to V_{CC} thus forcing a logic "0" to the inputs of AND gates G2 and G3. The 8238 has the connection to V_{CC}. This forces a logic "1" to AND gates G2 and G3 which allows $\overline{\text{IOW}}$ and $\overline{\text{MEMW}}$ to be advanced. This circuitry is internal to the devices and cannot be altered once the part has been fabricated.

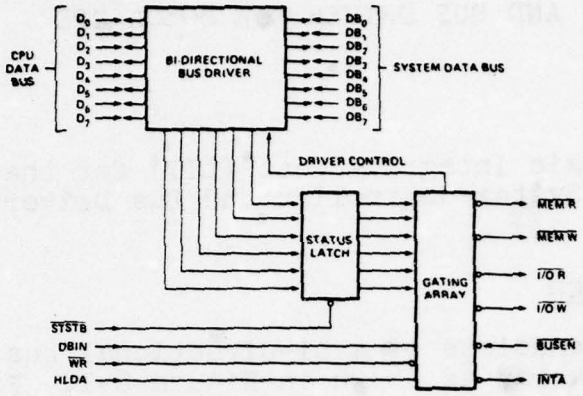


Figure 6-1. 8228 block diagram

Circuit Analysis and Vector Generation

Figure 6-4a shows the logic diagram for the PU flip-flop of Figure 6-2. The remaining flip-flops in the status latch are of the type shown in Figure 6-4b. The PU flip-flop is different from the others in that it has a clear input which functions as follows:

1. When clear is set to a logic "0", the Q-output will be set to a logic "0" independent of what was on the output of G7.

2. If clock is a logic "1" and clear is set back to a logic "1", the Q-output will return to the state of the D input.

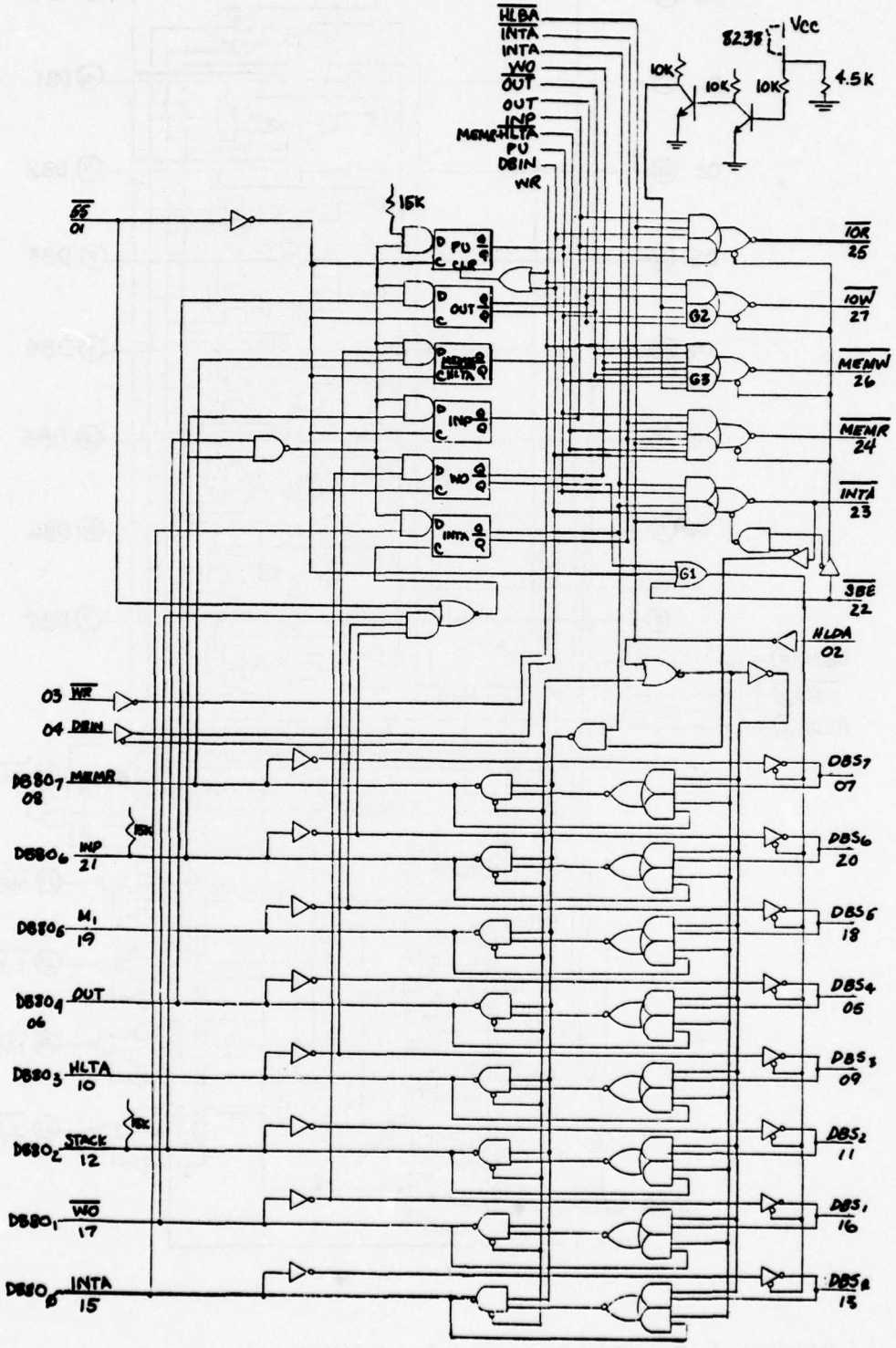
3. If clock is a logic "0" and the clear is set back to a logic "1", the Q-output will remain in the logic "0" state.

The vectors which were generated for the flip-flops verify the following:

1. Data is transferred to the output when the clock is high.

2. Changing the D input when the clock is low does not affect the output.

3. That each flip-flop can make the 0→0, 0→1, 1→1, and 1→0 transitions.


HLDA
INTA
INTA
WO
OUT
OUT
INP
MEMR
HLTA
PU
DBIN
WR
8238
Vcc
10K
10K
10K
4.5K
15K
01
PU
OUT
INP
WO
INTA
G1
G2
G3
IOR
25
IOW
27
MEMW
26
MEMR
24
INTA
23
SBE
22
HLDA
02
03 WR
04 DBIN
DBSO7 MEMR 08
DBSO6 INP 21
DBSO5 M1 19
DBSO4 OUT 06
DBSO3 HLTA 10
DBSO2 STACK 12
DBSO1 WO 17
DBSO0 INTA 15
DBS7 07
DBS6 20
DBS5 18
DBS4 06
DBS3 09
DBS2 11
DBS1 16
DBS0 13

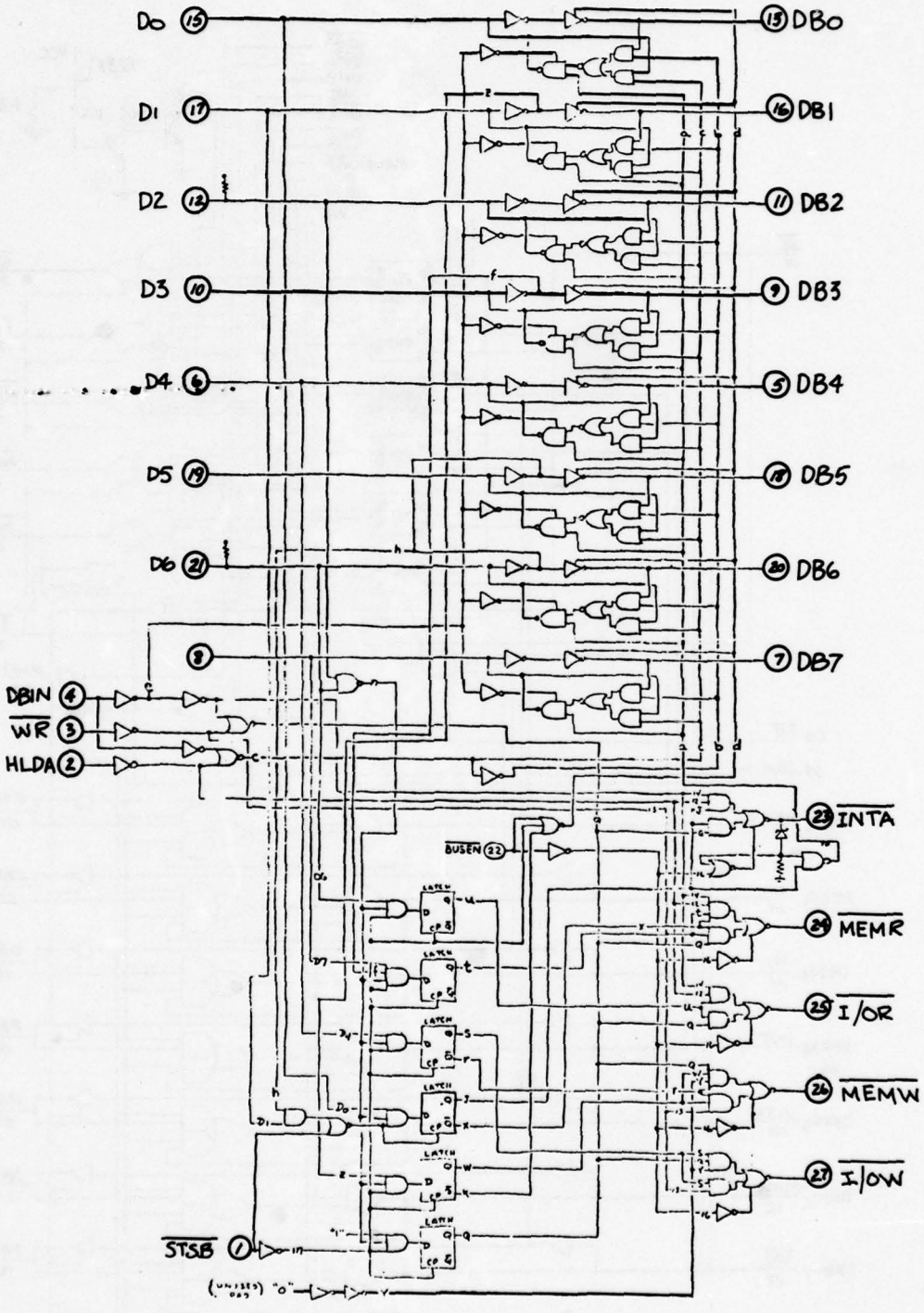
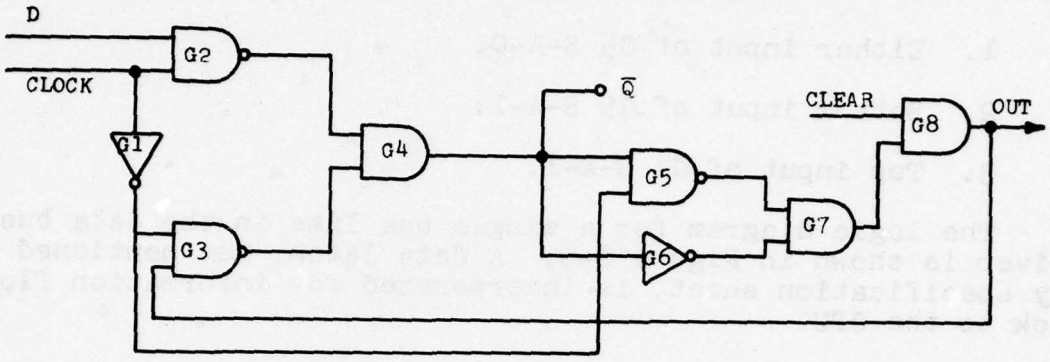
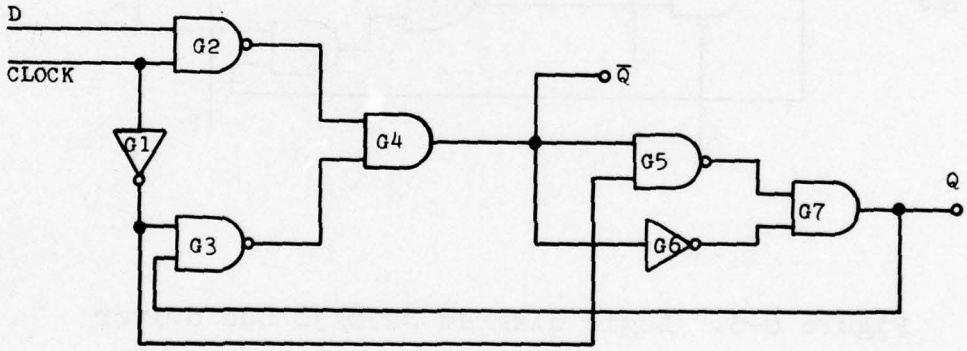


Figure 6-3. Vendor B's 8228/38 Logic Diagram



a



b

Figure 6-4. Flip-flop logic diagram

This verification detects all possible stuck-at faults in the implementation shown in Figure 6-2. It is not possible to detect the following faults:

1. Either input of G5 S-A-0.

2. Bottom input of G5 S-A-1.

3. Top input of G7 S-A-1.

The logic diagram for a single bus line in the data bus driver is shown in Figure 6-5. A data latch, not mentioned in any specification sheet, is incorporated for information flowing back to the CPU.

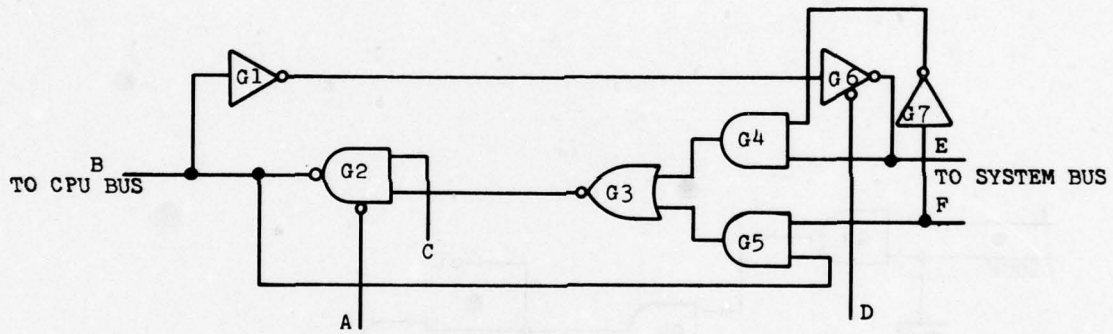


Figure 6-5. Logic diagram 8228/38 bus driver

The set of vectors (see Table 6-1) developed for the bi-directional bus driver detect all possible stuck-at faults in the implementation shown. It is not possible to detect the upper input of G5 S-A-1.

A	B	C	D	E	F
0	0	1	1	0	0
0	1	0	1	0	0
0	0	1	1	0	1
0	0	1	1	1	1
0	1	1	1	1	0
1	*	1	1	1	0
0	1	1	1	1	1
0	1	1	1	0	1
0	0	1	1	0	0
1	*	1	1	0	0
1	0	X	0	0	X
1	1	X	0	1	X
1	0	X	1	*	X
1	1	X	1	*	*

X = Don't Care
* = Measure High Impedance

Table 6-1. Bus driver vectors

A logic integrity test for the complete device was then developed. This effort consisted of ensuring that the vectors applicable to a single stage were applied to each stage of the system controller and that a failure would be propagated to the output. The test vectors required to test the 8228 and 8238 are shown in Tables 6-2 and 6-3, respectively. These vectors provide a 100% Test Confidence Level for Vendor A's and Vendor C's devices.

3260 Test

A test program was developed for a Tektronix 3260 automatic tester. This program functionally tests the device by applying the set of input vectors described above to the device and checking the resulting output states against the expected output vectors. The vectors were verified using devices from Vendor A and C.

Appendix A contains the wiring list for the socket card, load module schematic, copies of the test program, pin assignment program and test pattern files.

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																									MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	STSTB	HLDA	WR	DBIN	D04	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	D0	DB1	D1	DB5	D5	DB6	D6	BUSEN	INTA	MEMR	I/OR	MEMW	I/OW	Vcc		Min	Max	Min	Max	Min	Max	
7			1	B	X	X	B	X	X	X	X	X	X	X	X	X	GND	X	X	X	X	X	X	X	X	X	X	X	X	X	Vcc	ALL OUTPUTS						VDC
			2	B	A	A	B	Z	A	Z	A	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	L	H	L	H	H							
			3	B	A	A	B	Z	B	Z	B	Z	A	Z	A	Z		B	Z	B	Z	A	Z	B	B	H	H	H	H	H							
			4	B	A	A	B	Z	A	Z	A	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	L	H	L	H	H							
			5	B	A	B	B	Z	A	Z	A	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	H	H	H	H	L							
			6	B	A	A	B	Z	A	Z	A	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	L	H	L	H	H							
			7	A	A	A	B	H	A	H	A	L	B	L	B	H		A	L	B	L	B	H	A	B	L	H	L	H	H							
			8	A	A	A	B	H	A	H	A	L	B	H	A	H		A	L	B	L	B	H	A	B	L	H	L	H	H							
			9	A	A	B	B	H	A	H	A	L	B	H	A	H		A	L	B	L	B	H	A	B	H	H	H	H	L							
			10	A	A	A	B	H	A	H	A	L	B	H	A	H		A	L	B	L	B	H	A	B	H	H	H	H	H							
			11	B	A	A	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	A	Z	A	B	H	L	L	H	H							
			12	B	A	B	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	A	Z	A	B	H	H	H	L	H							
			13	B	A	A	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	A	Z	A	B	H	L	L	H	H							
			14	A	A	A	B	L	B	H	A	L	B	L	B	L		B	L	B	H	A	H	A	B	H	L	L	H	H							
			15	A	A	A	B	H	A	H	A	H	A	L	B	H		A	H	A	H	A	H	A	B	H	L	L	H	H							
			16	A	A	B	B	H	A	H	A	H	A	L	B	H		A	H	A	H	A	H	A	B	H	H	H	L	H							
			17	B	B	A	B	Z	B	Z	A	Z	A	Z	A	Z		B	Z	A	Z	A	Z	B	B	H	H	H	H	H							
			18	B	B	B	B	Z	B	Z	A	Z	A	Z	A	Z		B	Z	A	Z	A	Z	B	B	H	H	H	H	H							
			19	B	B	A	B	Z	B	Z	A	Z	A	Z	A	Z		B	Z	A	Z	A	Z	B	B	H	H	H	H	H							
7			20	A	B	A	B	Z	B	Z	A	Z	A	Z	A	Z	GND	B	Z	A	Z	A	Z	B	B	H	H	H	H	H	Vcc	ALL OUTPUTS						VDC

Table 6-2. Functional test for the 8228

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																										MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	$\overline{STSTB}$	HLDA	$\overline{WR}$	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	D0	DB1	D1	DB5	D5	DB6	D6	BUSEN	$\overline{INTA}$	MEMR	I/OR	MEMW	I/OW	Vcc		Min	Max	Min	Max	Min	Max	
7			21	A	B	A	B	Z	B	Z	A	Z	B	Z	B	Z	GND	B	Z	B	Z	B	Z	A	B	H	H	H	H	H	Vcc	ALL OUTPUTS						VDC
			22	A	B	B	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	B	Z	A	B	H	H	H	H	H							
			23	A	B	B	B	Z	A	Z	B	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	H	H	H	H	H							
			24	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	H	Z		Z	Z	Z	Z	Z	Z	H	B	H	H	H	H	H							
			25	A	B	B	A	Z	X	Z	X	Z	X	Z	X	Z		X	Z	X	Z	X	Z	X	B	H	H	H	H	H							
			26	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	B	H	H	H	H	H							
			27	B	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	B	Z	B	B	H	H	H	H	L							
			28	B	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	B	Z	A	B	H	H	H	H	H							
			29	B	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	B	Z	B	B	H	H	H	H	L							
			30	B	B	B	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	B	Z	A	B	H	H	H	L	H							
			31	B	B	B	B	Z	B	Z	A	Z	B	Z	A	Z		B	Z	B	Z	B	Z	A	B	H	H	H	H	H							
			32	B	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	A	Z	A	B	H	H	H	H	H							
			33	A	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	A	Z	A	B	H	H	H	H	H							
			34	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	B	H	H	H	H	H							
			35	A	B	B	A	Z	X	Z	X	Z	X	Z	X	Z		X	Z	X	Z	X	Z	X	B	H	H	H	H	H							
			36	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	B	H	H	H	H	H							
			37	B	B	B	B	Z	B	Z	A	Z	B	Z	A	Z		B	Z	B	Z	B	Z	A	B	H	H	H	H	H							
			38	B	B	B	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	B	Z	A	B	H	H	H	L	H							
			39	B	B	B	B	Z	B	Z	A	Z	A	Z	B	Z		B	Z	A	Z	B	Z	B	B	H	H	H	H	H							
7			40	B	B	A	B	Z	B	Z	A	Z	A	Z	B	Z	GND	B	Z	A	Z	B	Z	B	B	H	H	H	H	H	Vcc	ALL OUTPUTS						VDC

Table 6-2. Functional test for the 8228

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																										MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	$\overline{SYSTB}$	HLDA	$\overline{WR}$	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	D0	DB1	D1	DB5	D5	DB6	D6	$\overline{BUSEN}$	$\overline{INTA}$	MEMR	I/OR	MEMW	$\overline{I/OW}$	Vcc		Min	Max	Min	Max	Min	Max	
7			41	B	B	A	B	Z	B	Z	A	Z	B	Z	B	Z	GND	B	Z	A	Z	B	Z	B	B	H	L	H	H	H	Vcc	ALL OUTPUTS						VDC
			42	B	B	A	B	Z	B	Z	B	Z	B	Z	B	Z		B	Z	A	Z	B	Z	B	B	H	H	H	H	H								
			43	B	B	A	B	Z	B	Z	B	Z	B	Z	A	Z		A	Z	B	Z	B	Z	B	B	L	H	H	H	H								
			44	B	B	A	B	Z	B	Z	B	Z	B	Z	A	Z		B	Z	B	Z	B	Z	B	B	H	H	H	H	H								
			45	B	A	A	B	Z	B	Z	B	Z	B	Z	A	Z		B	Z	A	Z	B	Z	B	B	H	H	H	H	H								
			46	B	B	A	B	Z	B	Z	B	Z	B	Z	A	Z		A	Z	A	Z	B	Z	B	B	H	H	H	H	H								
			47	B	B	A	B	Z	B	Z	B	Z	B	Z	A	Z		A	Z	A	Z	A	Z	B	B	L	H	H	H	H								
			48	B	B	A	B	Z	B	Z	B	Z	B	Z	A	Z		A	Z	A	Z	B	Z	B	B	L	H	H	H	H								
			49	B	B	A	B	Z	B	Z	B	Z	B	Z	B	Z		B	Z	A	Z	B	Z	B	B	L	H	H	H	H								
			50	B	B	A	B	Z	B	Z	B	Z	B	Z	B	Z		B	Z	A	Z	B	Z	A	B	H	H	L	H	H								
			51	B	B	B	B	Z	A	Z	A	Z	B	Z	B	Z		B	Z	A	Z	A	Z	A	B	H	H	H	H	L								
			52	A	B	B	B	Z	A	Z	A	Z	B	Z	B	Z		B	Z	A	Z	A	Z	A	B	H	H	H	H	L								
			53	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	B	H	H	H	H	L								
			54	A	B	B	A	A	H	A	H	A	H	A	H	A		H	A	H	A	H	A	H	B	H	L	L	H	L								
			55	A	A	B	A	A	H	A	H	A	H	A	H	A		H	A	H	A	H	A	H	B	H	H	H	H	L								
			56	A	B	B	A	A	H	A	H	A	H	A	H	A		H	A	H	A	H	A	H	B	H	L	L	H	L								
			57	A	B	B	B	B	Z	A	Z	A	Z	B	Z	B		Z	A	Z	A	Z	B	Z	A	Z	Z	Z	Z	Z								
			58	A	B	B	B	A	Z	B	Z	B	Z	A	Z	A		Z	B	Z	B	Z	A	Z	A	Z	Z	Z	Z	Z								
			59	A	B	A	A	B	L	B	L	B	L	B	L	B		L	B	L	B	L	B	L	B	H	L	L	H	H								
7			60	A	B	A	A	A	H	B	L	A	H	A	H	B	GND	L	B	L	A	H	B	L	B	H	L	L	H	H	Vcc	ALL OUTPUTS						VDC

Table 6-2. Functional test for the 8228

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																										MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	$\overline{STSTB}$	HLDA	$\overline{WR}$	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	D0	DB1	D1	DB5	D5	DB6	D6	$\overline{BUSEN}$	$\overline{INTA}$	MEMR	I/$\overline{O}$R	MEMW	I/$\overline{O}$W	Vcc		Min	Max	Min	Max	Min	Max	
7			61	A	B	A	A	B	L	B	L	B	L	A	H	B	GND	L	A	H	B	L	B	L	B	H	L	L	H	H	Vcc	ALL OUTPUTS						VDC
			62	A	B	A	A	B	L	B	L	A	H	A	H	B		L	A	H	B	L	B	L	B	H	L	L	H	H								
			63	A	B	A	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	B	H	H	H	H	H								
			64	B	B	A	B	Z	B	Z	A	Z	A	Z	A	Z		A	Z	B	Z	A	Z	B	B	L	H	H	H	H								
			65	B	B	A	B	Z	B	Z	A	Z	A	Z	A	Z		A	Z	B	Z	A	Z	B	A	Z	Z	Z	Z	Z								
			66	A	B	A	B	L	B	H	A	H	A	H	A	H		A	L	B	H	A	L	B	B	L	H	H	H	H								
			67	A	B	A	B	H	A	H	A	H	A	H	A	H		A	H	A	H	A	H	A	B	L	H	H	H	H								
			68	A	B	B	B	H	A	H	A	H	A	H	A	H		A	H	A	H	A	H	A	B	H	H	H	L	H								
			69	A	B	B	B	L	B	L	B	L	B	L	B	L		B	L	B	L	B	L	B	B	H	H	H	L	H								
			70	A	A	B	B	L	B	H	A	L	B	L	B	L		B	H	A	H	A	H	A	B	H	H	H	L	H								
			71	A	A	B	B	X	Z	X	Z	X	Z	X	Z	X		Z	X	Z	X	Z	X	Z	B	H	H	H	L	H								
			72	A	A	B	A	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	B	H	H	H	L	H								
			73	A	A	B	A	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	A	Z	Z	Z	Z	Z								
			74	A	B	B	B	X	Z	X	Z	X	Z	X	Z	X		Z	X	Z	X	Z	X	Z	B	H	H	H	L	H								
			75	B	B	A	B	Z	B	Z	A	Z	B	Z	B	Z		A	Z	B	Z	A	Z	A	B	L	H	L	H	H								
			76	A	B	A	B	L	B	H	A	L	B	L	B	H		A	L	B	H	A	H	A	B	L	H	L	H	H								
			77	A	B	A	B	X	Z	X	Z	X	Z	X	Z	X		Z	X	Z	X	Z	X	Z	B	L	H	L	H	H								
			78	A	B	A	A	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	B	L	H	L	H	H								
			79	A	A	A	B	X	Z	X	Z	X	Z	X	Z	X		Z	X	Z	X	Z	X	Z	B	H	H	H	H	H								
7			80	A	A	A	A	X	X	X	X	X	X	X	X	X	GND	X	X	X	X	X	X	X	B	H	H	H	H	H	Vcc	ALL OUTPUTS						VDC

Table 6-2. Functional test for the 8228

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																										MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	$\overline{STSTB}$	HLDA	$\overline{WR}$	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	D0	DB1	D1	DB5	D5	DB6	D6	BUSEN	$\overline{INTA}$	MEMR	$\overline{I/OR}$	MEMW	$\overline{I/OW}$	Vcc		Min	Max	Min	Max	Min	Max	
7			81	A	B	A	B	X	Z	X	Z	X	Z	X	Z	X	GND	Z	X	Z	X	Z	X	Z	B	H	H	H	H	H	Vcc	ALL OUTPUTS						VDC
			82	B	B	A	B	Z	A	Z	A	Z	B	Z	A	Z		B	Z	B	Z	A	Z	B	B	H	L	H	H	H							
			83	A	B	A	B	H	A	H	A	L	B	H	A	L		B	L	B	H	A	L	B	B	H	L	H	H	H							
			84	A	B	A	B	X	Z	X	Z	X	Z	X	Z	X		Z	X	Z	X	Z	X	Z	B	H	L	H	H	H							
			85	A	B	A	A	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	B	H	L	H	H	H							
			86	A	A	A	A	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	B	H	H	H	H	H							
			87	A	B	A	B	X	Z	X	Z	X	Z	X	Z	X		Z	X	Z	X	Z	X	Z	B	H	H	H	H	H							
			88	B	B	A	A	A	H	B	L	B	L	A	H	A		H	B	L	B	L	A	H	A	Z	Z	Z	Z	Z							
			89	B	A	A	A	A	H	B	L	B	L	A	H	A		H	B	L	B	L	A	H	A	Z	Z	Z	Z	Z							
			90	B	A	A	A	B	H	A	L	A	L	B	H	B		H	A	L	A	L	B	H	A	Z	Z	Z	Z	Z							
			91	B	B	A	A	B	L	A	H	A	H	B	L	B		L	A	H	A	H	B	L	A	Z	Z	Z	Z	Z							
			92	B	A	A	A	B	L	A	H	A	H	B	L	B		L	A	H	A	H	B	L	A	Z	Z	Z	Z	Z							
			93	B	A	A	A	A	L	B	H	B	H	A	L	A		L	B	H	B	H	A	L	A	Z	Z	Z	Z	Z							
			94	B	B	A	A	A	H	B	L	B	L	A	H	A		H	B	L	B	L	A	H	A	Z	Z	Z	Z	Z							
			95	B	B	A	A	B	L	B	L	B	L	B	L	A		H	B	L	B	L	B	L	A	Z	Z	Z	Z	Z							
			96	A	B	A	A	B	L	B	L	B	L	B	L	A		H	B	L	B	L	B	L	A	Z	Z	Z	Z	Z							
			97	A	B	A	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	A	Z	Z	Z	Z	Z							
			98	A	B	A	B	Z	B	Z	A	Z	A	Z	B	Z		B	Z	A	Z	A	Z	B	A	Z	Z	Z	Z	Z							
			99	A	B	A	B	Z	A	Z	B	Z	B	Z	A	Z		A	Z	B	Z	B	Z	A	A	Z	Z	Z	Z	Z							
7			100	A	B	A	B	A	Z	B	Z	B	Z	A	Z	A	GND	Z	B	Z	B	Z	A	Z	A	Z	Z	Z	Z	Z	Vcc	ALL OUTPUTS						VDC

Table 6-2. Functional test for the 8228

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																										MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	STSTB	HLDA	WR	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	DO	DB1	D1	DB5	D5	DB6	D6	BUSEN	INTA	MEMR	I/OR	MEMW	I/OW	Vcc		Min	Max	Min	Max	Min	Max	
7			101	A	B	A	B	B	Z	A	Z	A	Z	B	Z	B	GND	Z	A	Z	A	Z	B	Z	A	Z	Z	Z	Z	Z	Vcc	ALL OUTPUTS						VDC
			102	A	B	A	A	B	L	B	L	B	L	B	L	B		L	B	L	B	L	B	L	A	Z	Z	Z	Z	Z								
			103	A	B	A	A	B	H	B	H	B	H	B	H	B		H	B	H	B	H	B	H	A	+12V	Z	Z	Z	Z								
7			104	B	B	A	A	B	L	B	L	B	L	B	L	B	GND	L	B	L	B	L	B	L	A	+12V	Z	Z	Z	Z	Vcc	ALL OUTPUTS						VDC

NOTES:

1. A = 2.0V B = 0.8V
2. H = 3.3V Min. for D_0- D_7
   H = 2.4V Min. for all other outputs
   L = 0.5V Max. for all outputs
3. X = Don't Care
4. Z = High impedance state. It must be checked at every data point noted in subgroup 7:
   a. A forcing voltage and resulting current for outputs D_2 and D_6 must meet the table below:

Forcing Voltage	Limit for Resulting Current
0.4V	-750uA Max.
5.5V	100uA Max.

   b. For all other high impedance outputs (excluding D_2 and D_6) either of two test procedures may be followed:

(1) A forcing voltage and the resulting current must meet the table below:

Pins	Forcing Voltage	Limit for Resulting Current
DB_0-DB_7;D_0; D_1;D_3-D_5;D_7	0.4V	-250uA Max.
DB_0-DB_7	5.5V	20uA Max.
D_0; D_1; D_3-D_5; D_7	5.5V	100uA Max.

(2) A load as shown below is connected to the outputs. The output voltage shall be measured from 70us to 100us after the high impedance control line is enabled. The resultant voltage at the output pin shall be: $1.0V \leq V_{out} \leq 2.0V$

OUTPUT	R1	RL
D_0,D_1,D_3-5,D_7	332KΩ $\pm$ 5%	536Ω $\pm$ 5%
DB_0-DB_7	237KΩ $\pm$ 5%	105Ω $\pm$ 5%

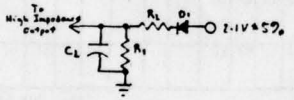


Table 6-2. Functional test for the 8228

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																											MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	$\overline{SYSTB}$	HLDA	$\overline{WR}$	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	DO	DB1	D1	DB5	D5	DB6	D6	BUSEN	$\overline{INTA}$	$\overline{MEMR}$	I/$\overline{OR}$	$\overline{MEMW}$	I/$\overline{OW}$	Vcc		Min	Max	Min	Max	Min	Max	
7			1	B	X	X	B	X	X	X	X	X	X	X	X	X	GND	X	X	X	X	X	X	X	X	X	X	X	X	X	Vcc	ALL OUTPUTS						VDC
			2	B	A	A	B	Z	A	Z	A	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	L	H	L	H	L							
			3	B	A	A	B	Z	B	Z	B	Z	A	Z	A	Z		B	Z	B	Z	A	Z	B	B	H	H	H	L	H							
			4	B	A	A	B	Z	A	Z	A	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	L	H	L	H	L							
			5	B	A	B	B	Z	A	Z	A	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	H	H	H	H	L							
			6	B	A	A	B	Z	A	Z	A	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	L	H	L	H	L							
			7	A	A	A	B	H	A	H	A	L	B	L	B	H		A	L	B	L	B	H	A	B	L	H	L	H	L							
			8	A	A	A	B	H	A	H	A	L	B	H	A	H		A	L	B	L	B	H	A	B	L	H	L	H	L							
			9	A	A	B	B	H	A	H	A	L	B	H	A	H		A	L	B	L	B	H	A	B	H	H	H	H	L							
			10	A	A	A	B	H	A	H	A	L	B	H	A	H		A	L	B	L	B	H	A	B	H	H	H	L	H							
			11	B	A	A	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	A	Z	A	B	H	L	L	H	H							
			12	B	A	B	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	A	Z	A	B	H	H	H	L	H							
			13	B	A	A	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	A	Z	A	B	H	L	L	L	H							
			14	A	A	A	B	L	B	H	A	L	B	L	B	L		B	L	B	H	A	H	A	B	H	L	L	L	H							
			15	A	A	A	B	H	A	H	A	H	A	L	B	H		A	H	A	H	A	H	A	B	H	L	L	L	H							
			16	A	A	B	B	H	A	H	A	H	A	L	B	H		A	H	A	H	A	H	A	B	H	H	H	L	H							
			17	B	B	A	B	Z	B	Z	A	Z	A	Z	A	Z		B	Z	A	Z	A	Z	B	B	H	H	H	H	H							
			18	B	B	B	B	Z	B	Z	A	Z	A	Z	A	Z		B	Z	A	Z	A	Z	B	B	H	H	H	H	H							
			19	B	B	A	B	Z	B	Z	A	Z	A	Z	A	Z		B	Z	A	Z	A	Z	B	B	H	H	H	H	H							
7			20	A	B	A	B	Z	B	Z	A	Z	A	Z	A	Z	GND	B	Z	A	Z	A	Z	B	B	H	H	H	H	H	Vcc	ALL OUTPUTS						VDC

Table 6-3. Functional test for the 8238

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																											MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	STSTB	HLDA	WR	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	DO	DB1	D1	DB5	D5	DB6	D6	BUSEN	INTA	MEMR	I/OR	MEMW	I/OW	Vcc		Min	Max	Min	Max	Min	Max	
7			21	A	B	A	B	Z	B	Z	A	Z	B	Z	B	Z	GND	B	Z	B	Z	B	Z	A	B	H	H	H	H	H	Vcc	ALL OUTPUTS						VDC
			22	A	B	B	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	B	Z	A	B	H	H	H	H	H								
			23	A	B	B	B	Z	A	Z	B	Z	B	Z	B	Z		A	Z	B	Z	B	Z	A	B	H	H	H	H	H								
			24	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	H	Z		Z	Z	Z	Z	Z	Z	H	B	H	H	H	H	H								
			25	A	B	B	A	Z	X	Z	X	Z	X	Z	X	Z		X	Z	X	Z	X	Z	X	B	H	H	H	H	H								
			26	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	B	H	H	H	H	H								
			27	B	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	B	Z	B	B	H	H	H	H	L								
			28	B	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	B	Z	A	B	H	H	H	H	H								
			29	B	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	B	Z	B	B	H	H	H	H	L								
			30	B	B	B	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	B	Z	A	B	H	H	H	L	H								
			31	B	B	B	B	Z	B	Z	A	Z	B	Z	A	Z		B	Z	B	Z	B	Z	A	B	H	H	H	H	H								
			32	B	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	A	Z	A	B	H	H	H	H	H								
			33	A	B	B	B	Z	A	Z	A	Z	B	Z	A	Z		A	Z	B	Z	A	Z	A	B	H	H	H	H	H								
			34	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	B	H	H	H	H	H								
			35	A	B	B	A	Z	X	Z	X	Z	X	Z	X	Z		X	Z	X	Z	X	Z	X	B	H	H	H	H	H								
			36	A	B	B	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	B	H	H	H	H	H								
			37	B	B	B	B	Z	B	Z	A	Z	B	Z	A	Z		B	Z	B	Z	B	Z	A	B	H	H	H	H	H								
			38	B	B	B	B	Z	B	Z	A	Z	B	Z	B	Z		B	Z	B	Z	B	Z	A	B	H	H	H	L	H								
			39	B	B	B	B	Z	B	Z	A	Z	A	Z	B	Z		B	Z	A	Z	B	Z	B	B	H	H	H	H	H								
7			40	B	B	A	B	Z	B	Z	A	Z	A	Z	B	Z	GND	B	Z	A	Z	B	Z	B	B	H	H	H	H	H	Vcc	ALL OUTPUTS						VDC

Table 6-3. Functional test for the 8238

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																										MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	$\overline{SSTB}$	HLDA	$\overline{WR}$	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	DO	DB1	D1	DB5	D5	DB6	D6	$\overline{BUSEN}$	$\overline{INTA}$	$\overline{MEMR}$	I/$\overline{OR}$	$\overline{MEMW}$	I/$\overline{OW}$	Vcc		Min	Max	Min	Max	Min	Max	
7			81	A	B	A	B	X	Z	X	Z	X	Z	X	Z	X	GND	Z	X	Z	X	Z	X	Z	B	H	H	H	H	H	Vcc	ALL OUTPUTS						VDC
			82	B	B	A	B	Z	A	Z	A	Z	B	Z	A	Z		B	Z	B	Z	A	Z	B	B	H	L	H	H	L							
			83	A	B	A	B	H	A	H	A	L	B	H	A	L		B	L	B	H	A	L	B	B	H	L	H	H	L							
			84	A	B	A	B	X	Z	X	Z	X	Z	X	Z	X		Z	X	Z	X	Z	X	Z	B	H	L	H	H	L							
			85	A	B	A	A	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	B	H	L	H	H	H							
			86	A	A	A	A	X	X	X	X	X	X	X	X	X		X	X	X	X	X	X	X	B	H	H	H	H	H							
			87	A	B	A	B	X	Z	X	Z	X	Z	X	Z	X		Z	X	Z	X	Z	X	Z	B	H	H	H	H	H							
			88	B	B	A	A	A	H	B	L	B	L	A	H	A		H	B	L	B	L	A	H	A	Z	Z	Z	Z	Z							
			89	B	A	A	A	A	H	B	L	B	L	A	H	A		H	B	L	B	L	A	H	A	Z	Z	Z	Z	Z							
			90	B	A	A	A	B	H	A	L	A	L	B	H	B		H	A	L	A	L	B	H	A	Z	Z	Z	Z	Z							
			91	B	B	A	A	B	L	A	H	A	H	B	L	B		L	A	H	A	H	B	L	A	Z	Z	Z	Z	Z							
			92	B	A	A	A	B	L	A	H	A	H	B	L	B		L	A	H	A	H	B	L	A	Z	Z	Z	Z	Z							
			93	B	A	A	A	A	L	B	H	B	H	A	L	A		L	B	H	B	H	A	L	A	Z	Z	Z	Z	Z							
			94	B	B	A	A	A	H	B	L	B	L	A	H	A		H	B	L	B	L	A	H	A	Z	Z	Z	Z	Z							
			95	B	B	A	A	B	L	B	L	B	L	B	L	A		H	B	L	B	L	B	L	A	Z	Z	Z	Z	Z							
			96	A	B	A	A	B	L	B	L	B	L	B	L	A		H	B	L	B	L	B	L	A	Z	Z	Z	Z	Z							
			97	A	B	A	B	Z	Z	Z	Z	Z	Z	Z	Z	Z		Z	Z	Z	Z	Z	Z	Z	A	Z	Z	Z	Z	Z							
			98	A	B	A	B	Z	B	Z	A	Z	A	Z	B	Z		B	Z	A	Z	A	Z	B	A	Z	Z	Z	Z	Z							
			99	A	B	A	B	Z	A	Z	B	Z	B	Z	A	Z		A	Z	B	Z	B	Z	A	A	Z	Z	Z	Z	Z							
7			100	A	B	A	B	A	Z	B	Z	B	Z	A	Z	A	GND	Z	B	Z	B	Z	A	Z	A	Z	Z	Z	Z	Z	Vcc	ALL OUTPUTS						VDC

Table 6-3. Functional test for the 8238

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN)																										MEASUREMENT TERMINAL	TEST LIMITS						UNITS
				1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28		Subgroup 1 T_A = 25°C		Subgroup 2 T_A = 125°C		Subgroup 3 T_A = -55°C		
			TEST NO.	$\overline{STSTB}$	HLDA	$\overline{WR}$	DBIN	DB4	D4	DB7	D7	DB3	D3	DB2	D2	DB0	GND	D0	DB1	D1	DB5	D5	DB6	D6	$\overline{BUSEN}$	$\overline{INTA}$	$\overline{MEMR}$	$\overline{I/OR}$	$\overline{MEMW}$	$\overline{I/OW}$	Vcc		Min	Max	Min	Max	Min	Max	
7			101	A	B	A	B	B	Z	A	Z	A	Z	B	Z	B	GND	Z	A	Z	A	Z	B	Z	A	Z	Z	Z	Z	Z	Vcc	ALL OUTPUTS						VDC
			102	A	B	A	A	B	L	B	L	B	L	B	L	B		L	B	L	B	L	B	L	A	Z	Z	Z	Z	Z							
			103	A	B	A	A	B	H	B	H	B	H	B	H	B		H	B	H	B	H	B	H	A	+12V	Z	Z	Z	Z							
↓ 7			104	B	B	A	A	B	L	B	L	B	L	B	L	B	GND	L	B	L	B	L	B	L	A	+12V	Z	Z	Z	Z	Vcc	ALL OUTPUTS						VDC

NOTES:

1. A = 2.0V B = 0.8V
2. H = 3.3V Min. for D_0- D_7
   H = 2.4V Min. for all other outputs
   L = 0.5V Max. for all outputs
3. X = Don't Care
4. Z = High impedance state. It must be checked at every data point noted in subgroup 7:
   a. A forcing voltage and resulting current for outputs D_2 and D_6 must meet the table below:

Forcing Voltage	Limit for Resulting Current
0.4V	-750uA Max.
5.5V	100uA Max.

   b. For all other high impedance outputs (excluding D_2 and D_6) either of two test procedures may be followed:

(1) A forcing voltage and the resulting current must meet the table below:

Pins	Forcing Voltage	Limit for Resulting Current
DB_0-DB_7; D_0; D_1; D_3-D_5; D_7	0.4V	-250uA Max.
DB_0-DB_7	5.5V	20uA Max.
D_0; D_1; D_3-D_5; D_7	5.5V	100uA Max.

(2) A load as shown below is connected to the outputs. The output voltage shall be measured from 70ns to 100ns after the high impedance control line is enabled. The resultant voltage at the output pin shall be: $1.0V \leq V_{out} \leq 2.0V$

OUTPUT	R1	RL
D_0,D_1,D_3-5,D_7	332KΩ±5%	536Ω±5%
DB_0-DB_7	237KΩ±5%	105Ω±5%

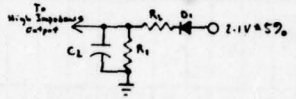


Table 6-3. Functional test for the 8238

SECTION VII

DEVELOPMENT OF A LOGIC INTEGRITY TEST FOR THE 8224 CLOCK GENERATOR AND DRIVER FOR THE 8080A CPU

Objective

Develop logic integrity tests for the 8224, clock generator and driver for the 8080A CPU.

Circuit Description

The 8224 is a single chip clock generator/driver for the 8080A CPU. It is controlled by a crystal, selected by the designer, to meet his particular system speed requirements. Figure 7-1 shows configuration, logic diagram and pin nomenclature.

Internal circuits are included to provide power-up reset, advance status strobe and synchronization of ready.

Circuit Investigation and Vector Generation

Before the 8224 test vectors could be generated, information not contained in the device specification sheets was requested and received from Vendor C. This information consisted of the timing relationship between Ø 1, Ø 1A, Ø 2 and Ø 2D (Figure 7-2) and a method of operating the chip without a crystal. The latter was required to simplify synchronization of the device with the test equipment being used. The method used consists of driving the XTAL 1 and XTAL 2 inputs with complimentary levels as shown in Figure 7-3. The phase of the oscillator output is related to the XTAL 1 and 2 inputs as shown in Figure 7-4.

The test vectors were developed using the timing information from Vendor C, lab data, and the 8224 logic diagram. An initialization procedure (Figure 7-5) was devised to reset all internal flip-flops and insure that the device input and output levels are always identical prior to vector 1.

3260 Test

A test program was developed for a Tektronix 3260 automatic tester. This program functionally tests the device by applying the set of input vectors described above to the device and checking the resulting output states against the expected output vectors. Appendix A contains the wiring list for the socket card, load module schematic, and copies of the test program, pin assignment program and test pattern file.

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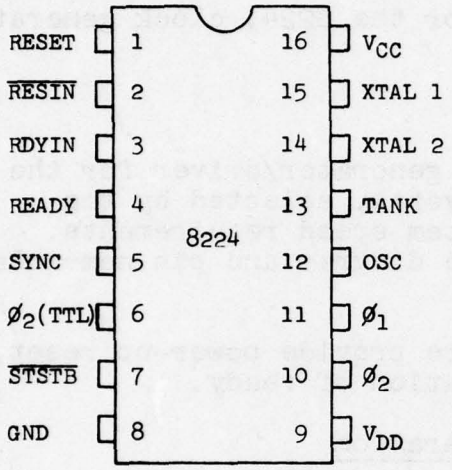
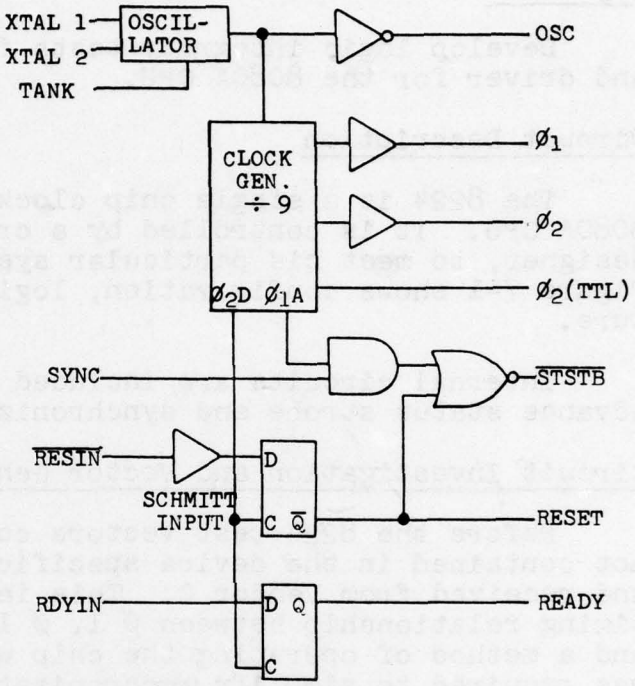
(A) Pin Configuration



(B) Logic Diagram



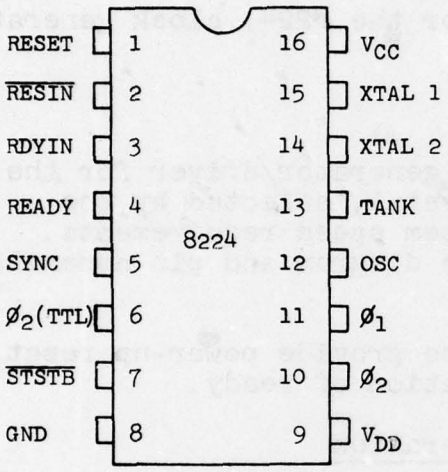
(C) Pin Names

RESIN	RESET INPUT
RESET	RESET OUTPUT
RDYIN	READY INPUT
READY	READY OUTPUT
SYNC	SYNC INPUT
STSTB	STATIS STB (ACTIVE LOW)
Ø1	8080 CLOCKS
Ø2	

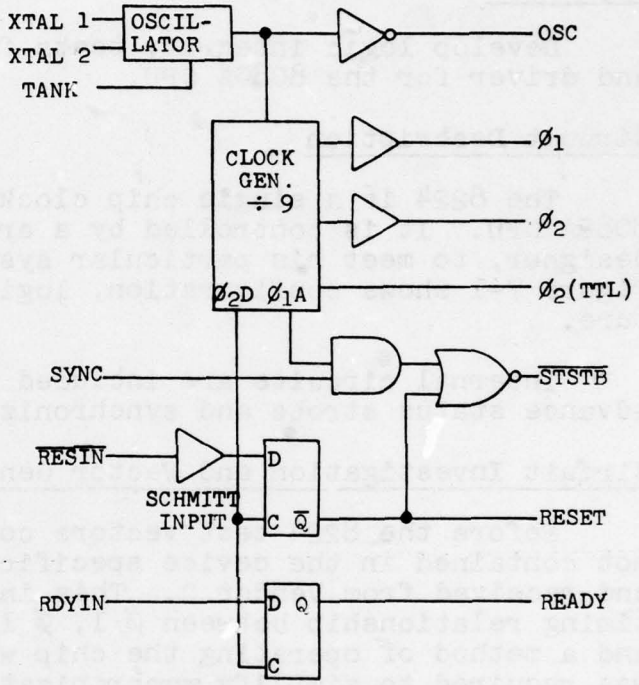
XTAL 1	CONNECTIONS FOR CRYSTAL
XTAL 2	
TANK	USED WITH OVERTONE XTAL
OSC	OSCILLATOR OUTPUT
Ø2 (TTL)	Ø2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

Figure 7-1. 8224 configuration, logic diagram and pin names

(A) Pin Configuration



(B) Logic Diagram



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OSC	OSCILLATOR OUTPUT
Ø2 (TTL)	Ø2 CLK (TTL LEVEL)
VCC	+5V
VDD	+12V
GND	0V

Figure 7-1. 8224 configuration, logic diagram and pin names

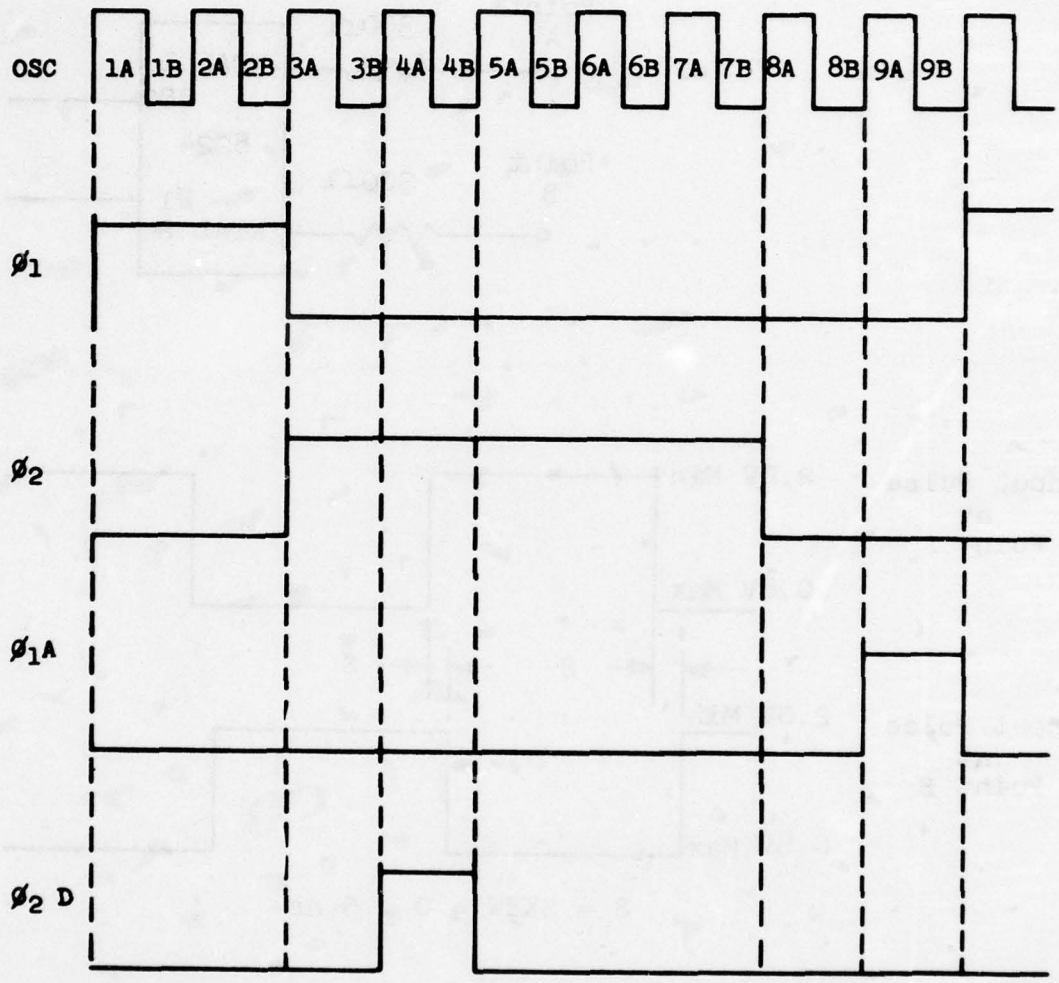

Figure 7-2. 8224 clock timing diagram

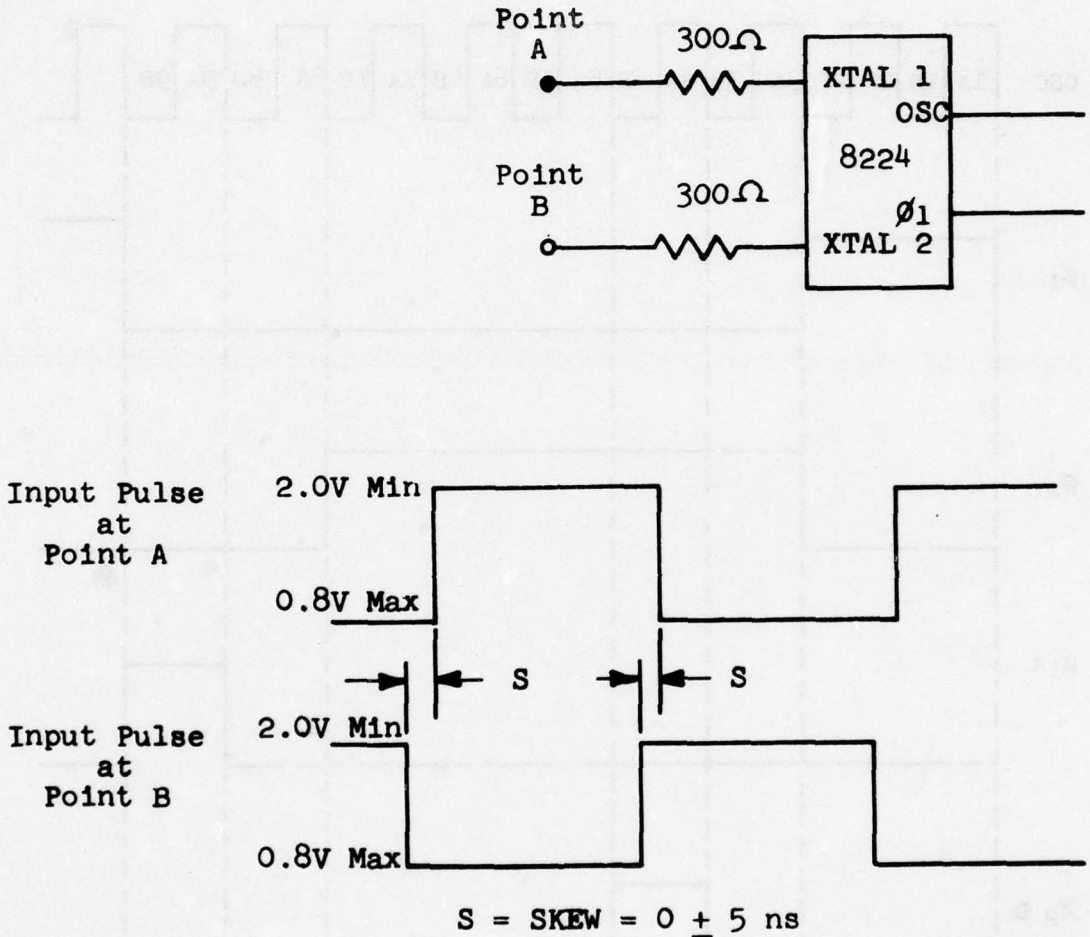

Figure 7-3. 8224 test circuit

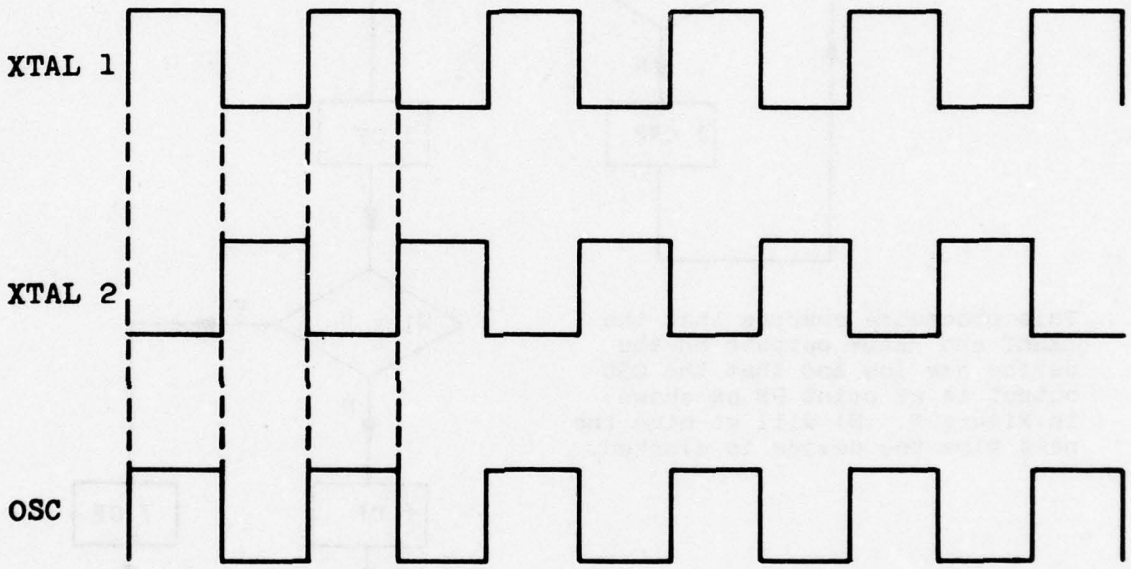

Figure 7-4. Oscillator input/output timing diagram

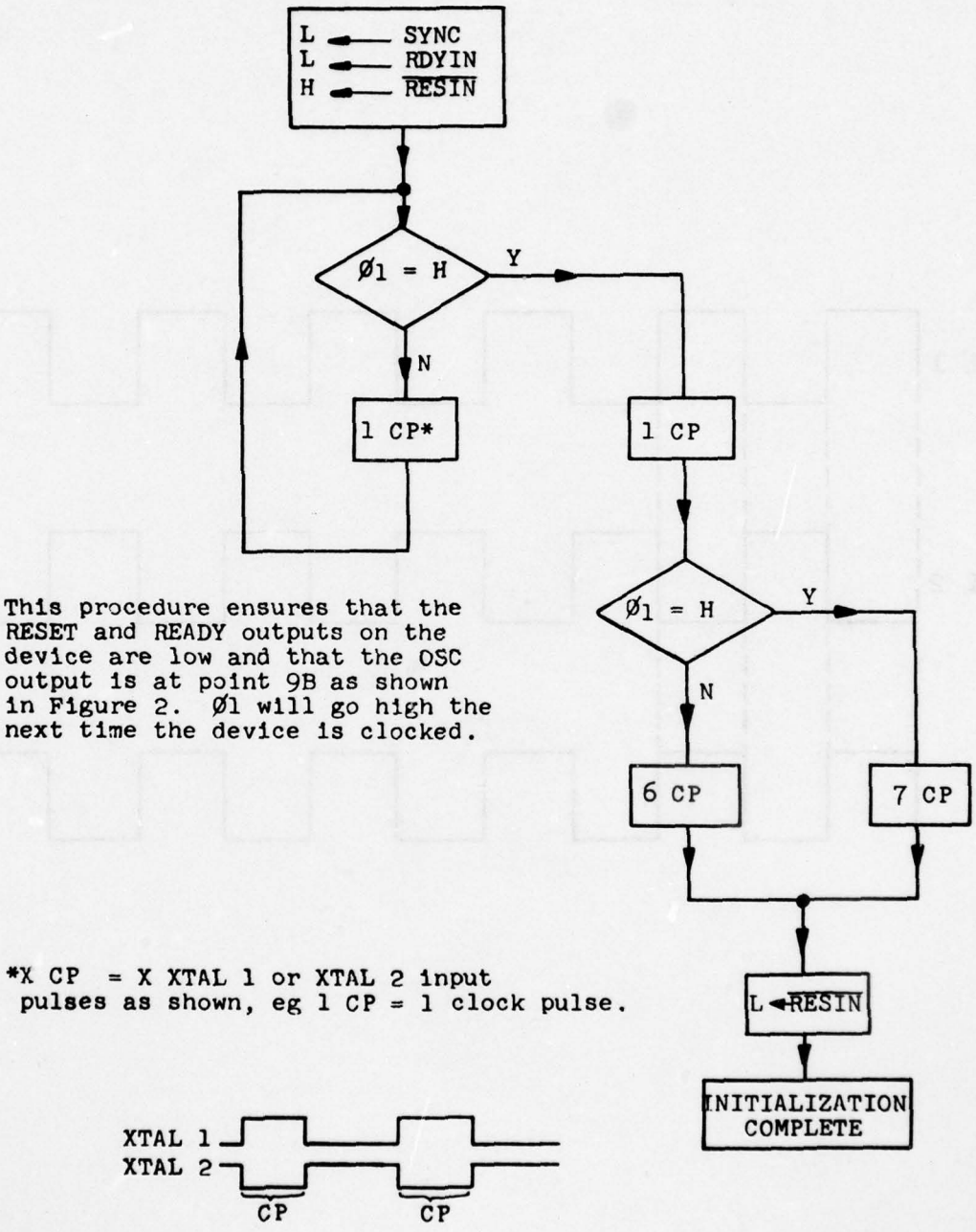

Figure 7-5. Initialization procedure

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN) 8224

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	MEASUREMENT TERMINAL	TEST LIMITS		
			TEST NO.	RESET	$\overline{\text{RESIN}}$	RDYIN	READY	SYNC	ϕ_2(TTL)	$\overline{\text{STSTB}}$	GND	V_{DD}	ϕ_2	ϕ_1	OSC	TANK	XTAL 2	XTAL 1	V_{CC}		MIN	MAX	UNITS
				INITIALIZATION PER FIGURE 5.																			
7	TRUTH TABLE TEST	3014	1	L	B	B	L	B	L	H	GND	10.8	L	H	H		B	A	4.5	All Outputs	H or L as shown		VDC
			2	L	B	B	L	B	L	H			L	H	L		A	B					
			3	L	B	B	L	B	L	H			L	H	H		B	A					
			4	L	B	B	L	B	L	H			L	H	L		A	B					
			5	L	B	B	L	B	H	H			H	L	H		B	A					
			6	L	B	B	L	B	H	H			H	L	L		A	B					
			7	H	B	B	L	B	H	L			H	L	H		B	A					
			8	H	B	B	L	B	H	L			H	L	L		A	B					
			9	H	B	B	L	B	H	L			H	L	H		B	A					
			10	H	B	B	L	B	H	L			H	L	L		A	B					
			11	H	B	B	L	B	H	L			H	L	H		B	A					
			12	H	B	B	L	B	H	L			H	L	L		A	B					
			13	H	B	B	L	B	H	L			H	L	H		B	A					
			14	H	B	B	L	B	H	L			H	L	L		A	B					
			15	H	B	B	L	B	L	L			L	L	H		B	A					
			16	H	B	B	L	B	L	L			L	L	I		A	B					
			17	H	B	B	L	A	L	L			L	L	H		B	A					
			18	H	B	B	L	A	L	L			L	L	L		A	B					
			19	H	B	A	L	A	L	L			L	H	H		B	A					
			20	H	B	A	L	A	L	L			L	H	L		A	B					
			21	H	B	A	L	A	L	L			L	H	H		B	A					
			22	H	B	A	L	A	L	L			L	H	L		A	B					
			23	H	B	A	L	A	H	L			L	L	H		B	A					
7			24	H	B	A	L	A	H	L	GND	10.8	H	L	L		A	B	4.5	All Outputs	H or L as shown		VDC

Table 7-1. Functional test for the 8224

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN) 8224

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	MEASUREMENT TERMINAL	TEST LIMITS		
			TEST NO.	RESET	$\overline{\text{RESIN}}$	RDYIN	READY	SYNC	ϕ_2(TTL)	$\overline{\text{STSTB}}$	GND	V_{DD}	ϕ_2	ϕ_1	OSC	TANK	XTAL 2	XTAL 1	V_{CC}		MIN	MAX	UNITS
7	TRUTH TABLE TEST	3014	25	H	B	A	H	A	H	L	GND	10.8	H	L	H		B	A	4.5	All Outputs	H	or L	VDC
			26	H	B	A	H	A	H	L			H	L	L		A	B			as	shown	
			27	H	B	A	H	A	H	L			H	L	H		B	A					
			28	H	B	A	H	A	H	L			H	L	L		A	B					
			29	H	A	A	H	A	H	L			H	L	H		B	A					
			30	H	A	A	H	A	H	L			H	L	L		A	B					
			31	H	A	A	H	A	H	L			H	L	H		B	A					
			32	H	A	A	H	A	H	L			H	L	L		A	B					
			33	H	A	A	H	A	L	L			L	L	H		B	A					
			34	H	A	A	H	A	L	L			L	L	L		A	B					
			35	H	A	A	H	A	L	L			L	L	H		B	A					
			36	H	A	A	H	A	L	L			L	L	L		A	B					
			37	H	A	A	H	A	L	L			L	H	H		B	A					
			38	H	A	A	H	A	L	L			L	H	L		A	B					
			39	H	A	A	H	A	L	L			L	H	H		B	A					
			40	H	A	A	H	A	L	L			L	H	L		A	B					
			41	H	A	A	H	A	H	L			H	L	H		B	A					
			42	H	A	A	H	A	H	L			H	L	L		A	B					
			43	L	A	A	H	A	H	H			H	L	H		B	A					
			44	L	B	B	H	A	H	H			H	L	L		A	B					
			45	L	B	B	H	A	H	H			H	L	H		B	A					
			46	L	B	B	H	A	H	H			H	L	L		A	B					
			47	L	A	A	H	A	H	H			H	L	H		B	A					
7			48	L	A	A	H	A	H	H	GND	10.8	H	L	L		A	B	4.5	All Outputs	H	or L	VDC
																					as	shown	

Table 7-1. Functional test for the 8224

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN) — 8224

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	MEASUREMENT TERMINAL	TEST LIMITS		
			TEST NO.	RESET	$\overline{RESIN}$	RDYIN	READY	SYNC	ϕ_2 (TTL)	$\overline{STSTB}$	GND	V_{DD}	ϕ_2	ϕ_1	OSC	TANK	XTAL2	XTAL1	V_{cc}		MIN	MAX	UNITS
7	TRUTH TABLE TEST	3014	49	L	A	A	H	A	H	H	GND	10.8	H	L	H		B	A	4.5	all outputs	H or L as shown		V_{IC}
			50	L	A	B	H	A	H	H			H	L	L		A	B					
			51	L	A	B	H	A	L	H			L	L	H		B	A					
			52	L	A	B	H	A	L	H			L	L	L		A	B					
			53	L	A	B	H	A	L	L			L	L	H		B	A					
			54	L	A	B	H	A	L	L			L	L	L		A	B					
			55	L	A	B	H	A	L	H			L	H	H		B	A					
			56	L	A	B	H	B	L	H			L	H	L		A	B					
			57	L	A	B	H	B	L	H			L	H	H		B	A					
			58	L	A	B	H	B	L	H			L	H	L		A	B					
			59	L	A	B	H	B	H	H			H	L	H		B	A					
			60	L	A	B	H	B	H	H			H	L	L		A	B					
			61	L	A	B	L	B	H	H			H	L	H		B	A					
			62	L	A	B	L	B	H	H			H	L	L		A	B					
			63	L	A	B	L	B	H	H			H	L	H		B	A					
			64	L	A	B	L	B	H	H			H	L	L		A	B					
			65	L	A	B	L	B	H	H			H	L	H		B	A					
			66	L	A	B	L	B	H	H			H	L	L		A	B					
			67	L	A	B	L	B	H	H			H	L	H		B	A					
			68	L	B	B	L	B	H	H			H	L	L		A	B					
			69	L	B	B	L	B	L	H			L	L	H		B	A					
			70	L	B	B	L	B	L	H			L	L	L		A	B					
			71	L	B	B	L	B	L	H			L	L	H		B	A					
7			72	L	B	B	L	B	L	H	GND	10.8	L	L	L		A	B	4.5	all outputs	H or L as shown		V_{DC}

Table 7-1. Functional test for the 8224

TERMINAL CONDITIONS (PINS NOT DESIGNATED ARE OPEN) 8224

SUBGROUP	SYMBOL	MIL-STD-883 METHOD	CASE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	MEASUREMENT TERMINAL	TEST LIMITS		
			TEST NO.	RESET	$\overline{RESIN}$	RDYIN	READY	SYNC	ϕ_2(TTL)	$\overline{STSTB}$	GND	V_{DD}	ϕ_2	ϕ_1	OSC	TANK	XTAL2	XTAL1	V_{CC}		MIN	MAX	UNITS
7	TRUTH	3014	73	L	B	B	L	B	L	H	GND	10.8	L	H	H		B	A	4.5	all	H or L		V_{DC}
↕	TABLE		74	L	B	B	L	B	L	H	↕	↕	L	H	L		A	B	↕	out-	as shown		↕
	TEST		75	L	B	B	L	B	L	H			L	H	H		B	A		puts	↕	↕	
			76	L	B	B	L	B	L	H			L	H	L		A	B		↕			
			77	L	B	B	L	B	H	H			H	L	H		B	A					
			78	L	B	B	L	B	H	H			H	L	L		A	B					
			79	H	B	B	L	B	H	L			H	L	H		B	A		all	H or L		V_{DC}
7			80	H	A	A	L	B	H	L	GND	10.8	H	L	L		A	B	4.5	out-	as shown		
																				puts			

NOTES:

1. Initialization per Figure 5 must precede functional test.
2. Tests must be performed in sequence given.
3. A = 2.6V for RESIN and 2.0V for all other inputs B = 0.8V
4. H = 9.0V min. for ϕ_1 and ϕ_2, 3.3V min. for READY and RESET, and 2.4V min. for all other outputs. L = 0.45V
5. Timing Waveforms

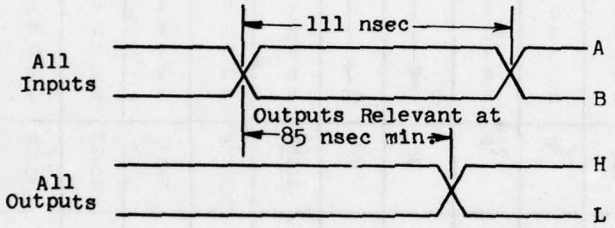

Table 7-1. Functional test for the 8224

SECTION VIII

GENERATION OF LOGIC INTEGRITY TESTS FOR THE 6821 PERIPHERAL INTERFACE ADAPTER

Objective

Develop Logic Integrity Tests for the 6821 Peripheral Interface Adapter.

Circuit Description

The Peripheral Interface Adapter (PIA) provides the universal means of interfacing peripheral equipment to the 6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes.

The block diagram for the 6821 is shown in Figure 8-1.

Vector Evaluation

Vendor G provided a logic diagram of the 6821 and a copy of their Fairchild Sentry test program which contained the functional tests for the device.

Descriptions of the Sentry tester and program language were obtained and studied to aid in the interpretation of the program for this device. This information will be useful in the future since virtually all manufacturers use Sentry testers and all programs supplied to RADC and GE are in Sentry format.

GE requested and received a better definition of some of the functional blocks used in the logic diagram and a description of the functional tests which indicated what portion of the logic was being checked by each vector. This description was helpful but it was not apparent when information was written into some of the registers. Therefore, a timing diagram was drawn to show the relationship between the inputs, outputs, and internal control signals.

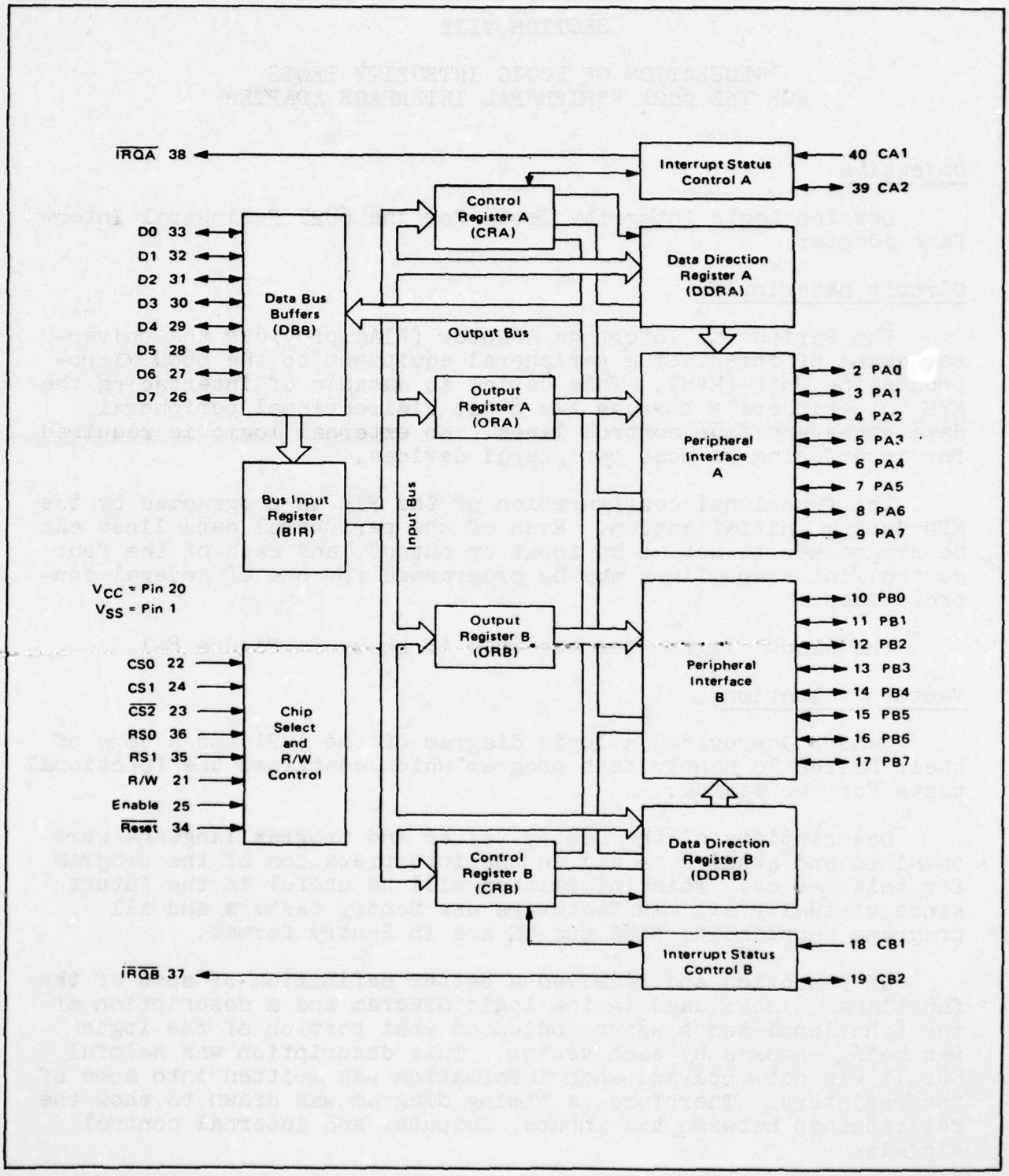

Figure 8-1. 6821 block diagram

It was then possible to determine, for each vector in the functional test, the contents of the internal registers, the data on the data and peripheral interface buses, and the direction in which the buses were transferring data. This information, which can be found in Appendix C, was necessary to check for register independence, bit independence, and cell integrity and to check the multiplexer which feeds the data bus. GE was in the process of using this information to determine the adequacy of the functional tests when it was learned that the 6821 is being redesigned. Although Vendor (G) stated that the functional test should not change very much, the evaluation was halted until the redesign is completed. When Vendor (G) submits this new information, GE will determine the impact on the functional test and the analysis.

This effort is continuing on another RADC characterization contract.

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